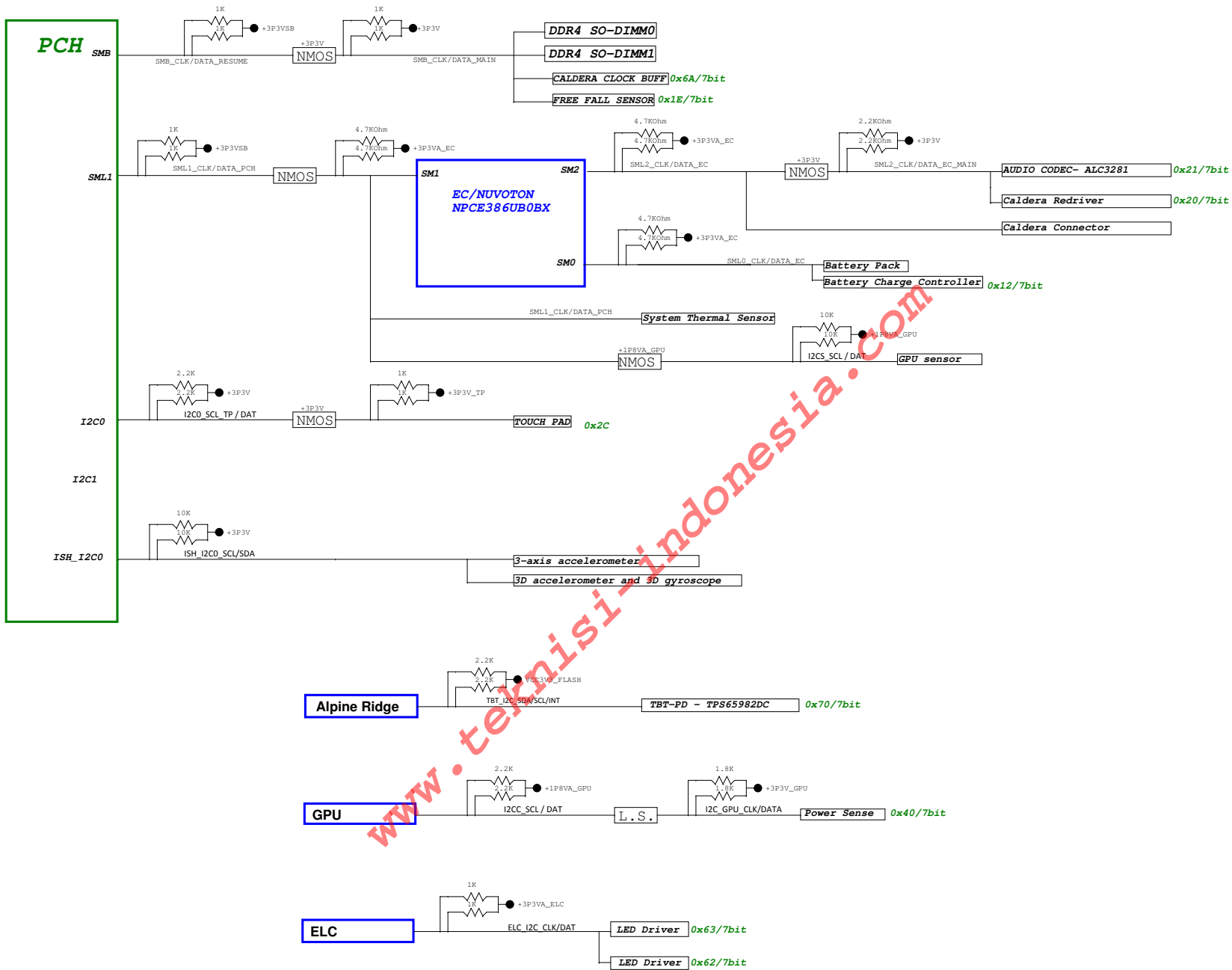


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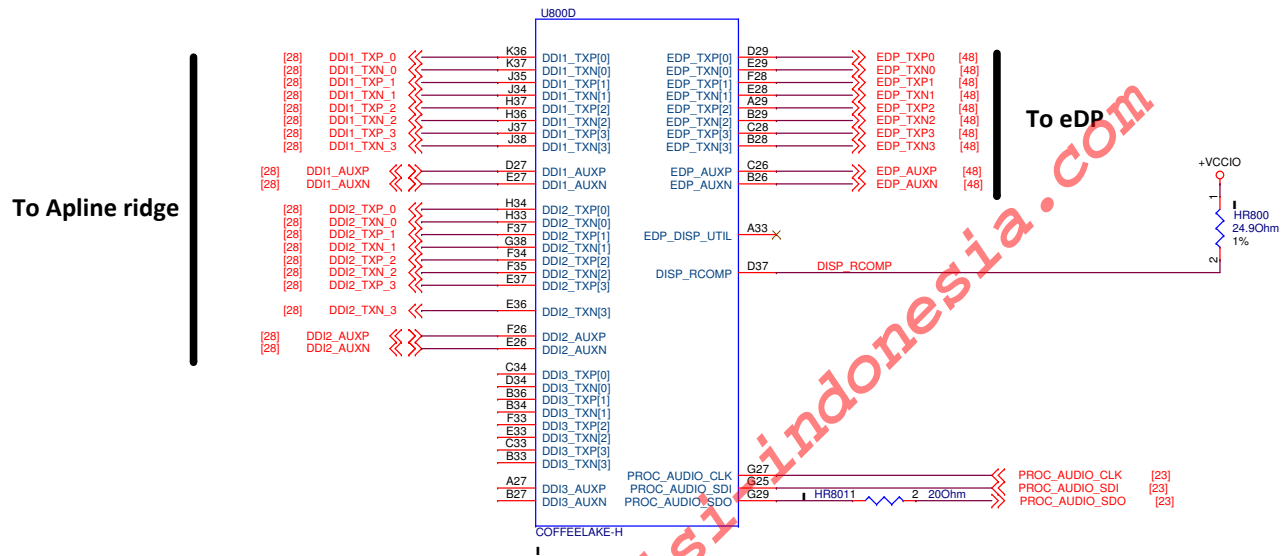
SMBUS & I2C Block Diagram



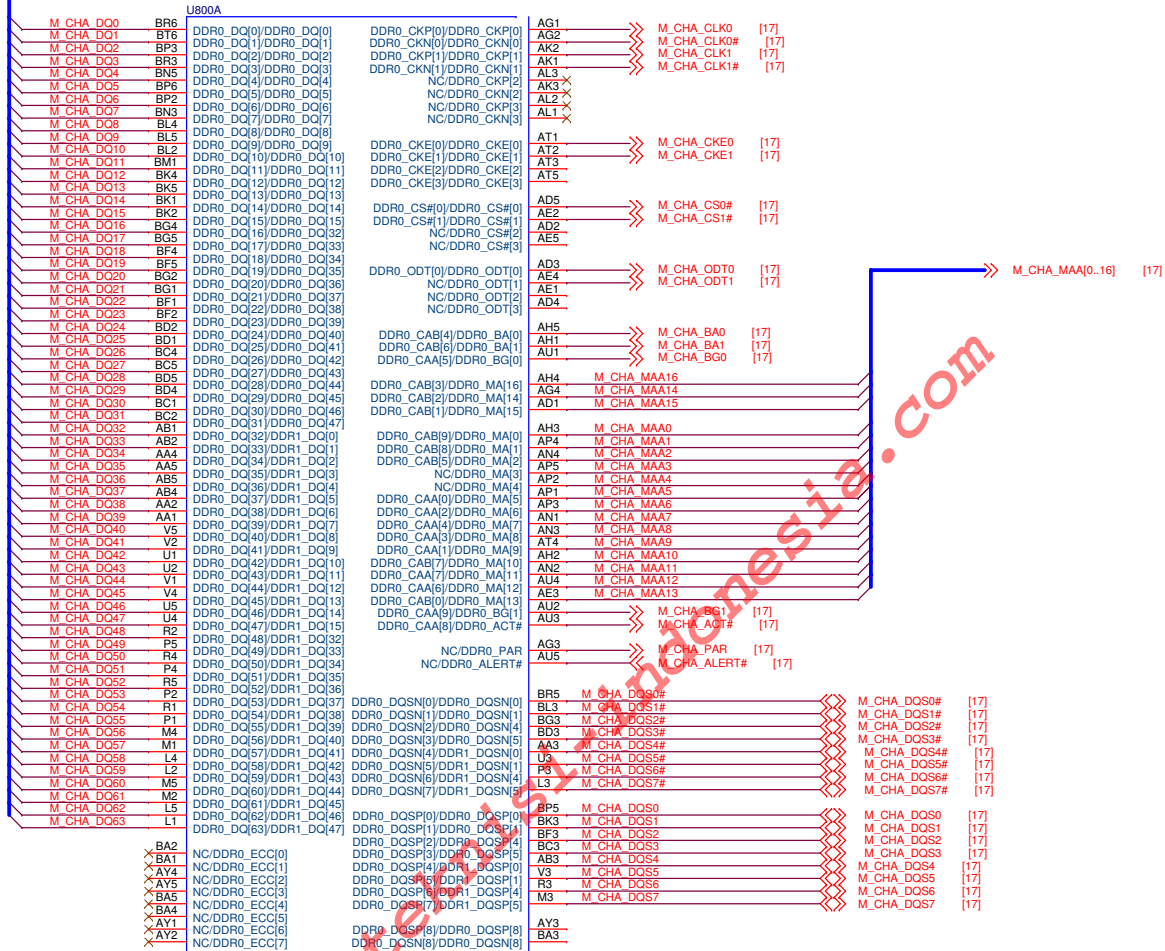
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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : POWER SEQUENCE	
Pegatron Corp		Engineer: Morris_chiu	
Size	Project Name		Rev
A2	Orion		1.0
Date: Monday, August 27, 2018		Sheet	7 of 88



[17] M_CHA_DQ[0..63] <<>



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU DDR4 CHA

Pegatron Corp. Engineer: Morris_chiu

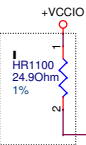
Size Project Name Orion Rev 1.0

Date: Monday, August 27, 2018 Sheet 9 of 93

Caldera x 4

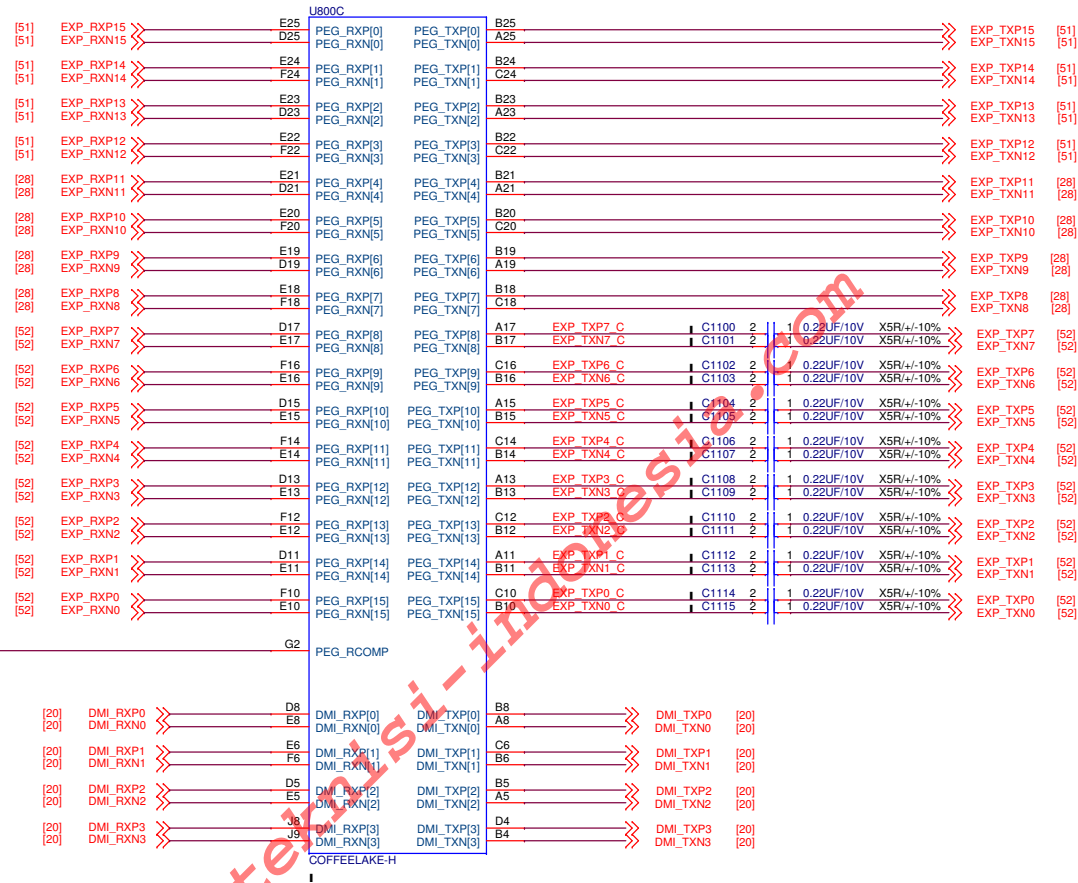
Alpine Ridge x 4

GPU x 8



NOTE:

W/S=12/15 mil, length<400mil



Caldera x 4

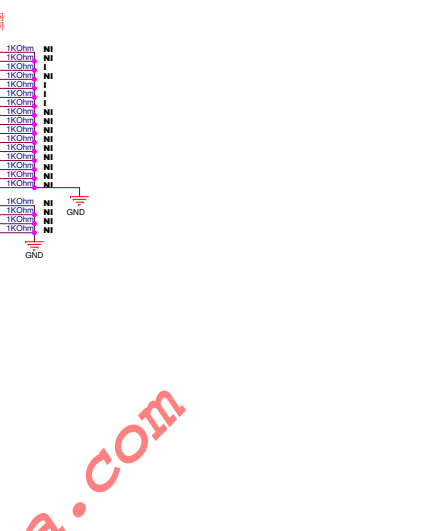
Alpine Ridge x 4

GPU x 8

PEGATRON DT-MB RESTRICTED SECRET

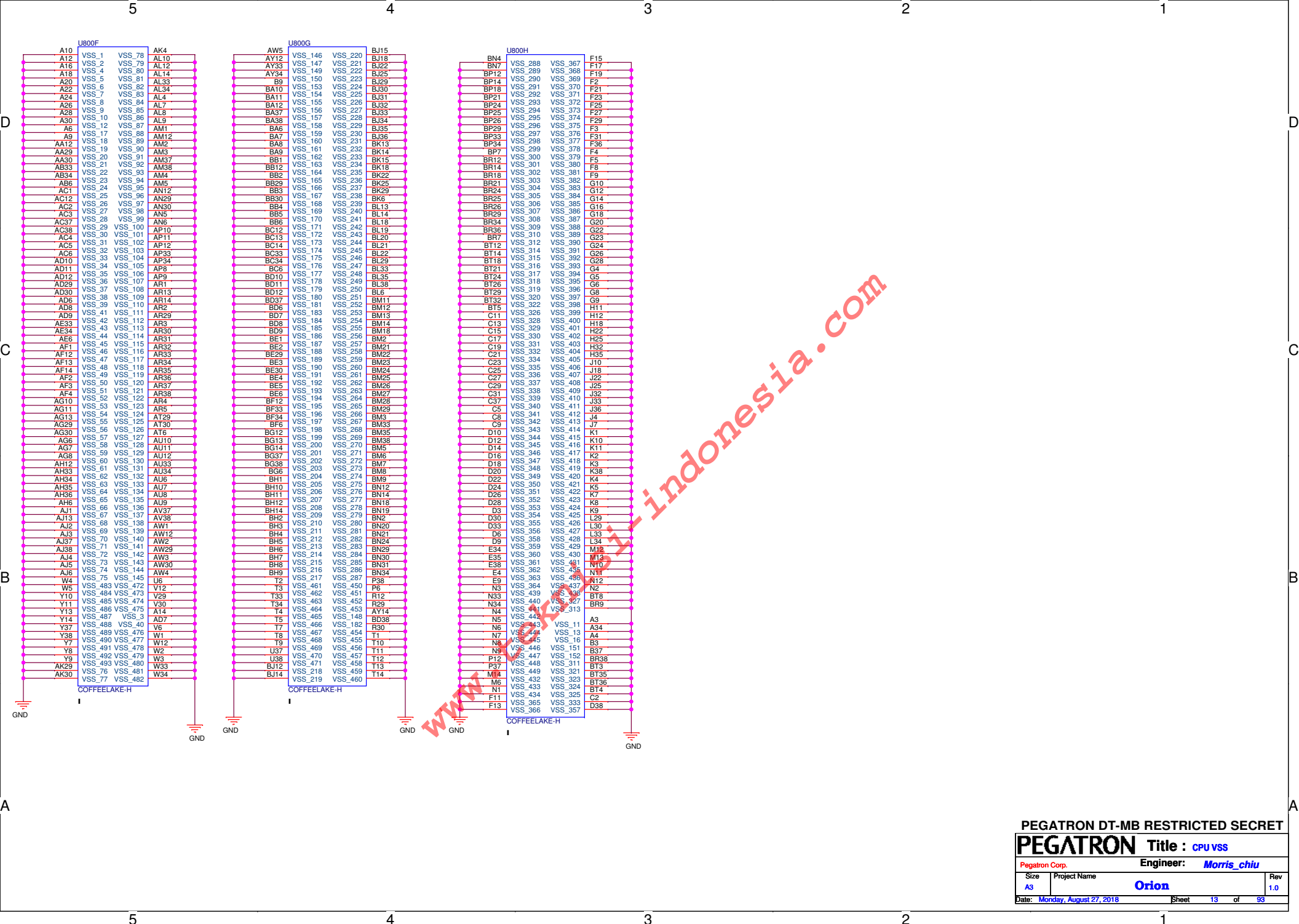
PEGATRON		Title : CPU PCIe/DMI	
Pegatron Corp.		Engineer: Morris_chiu	
Size	Project Name	Orion	Rev
A3			1.0
Date: Monday, August 27, 2018		Sheet	11 of 93

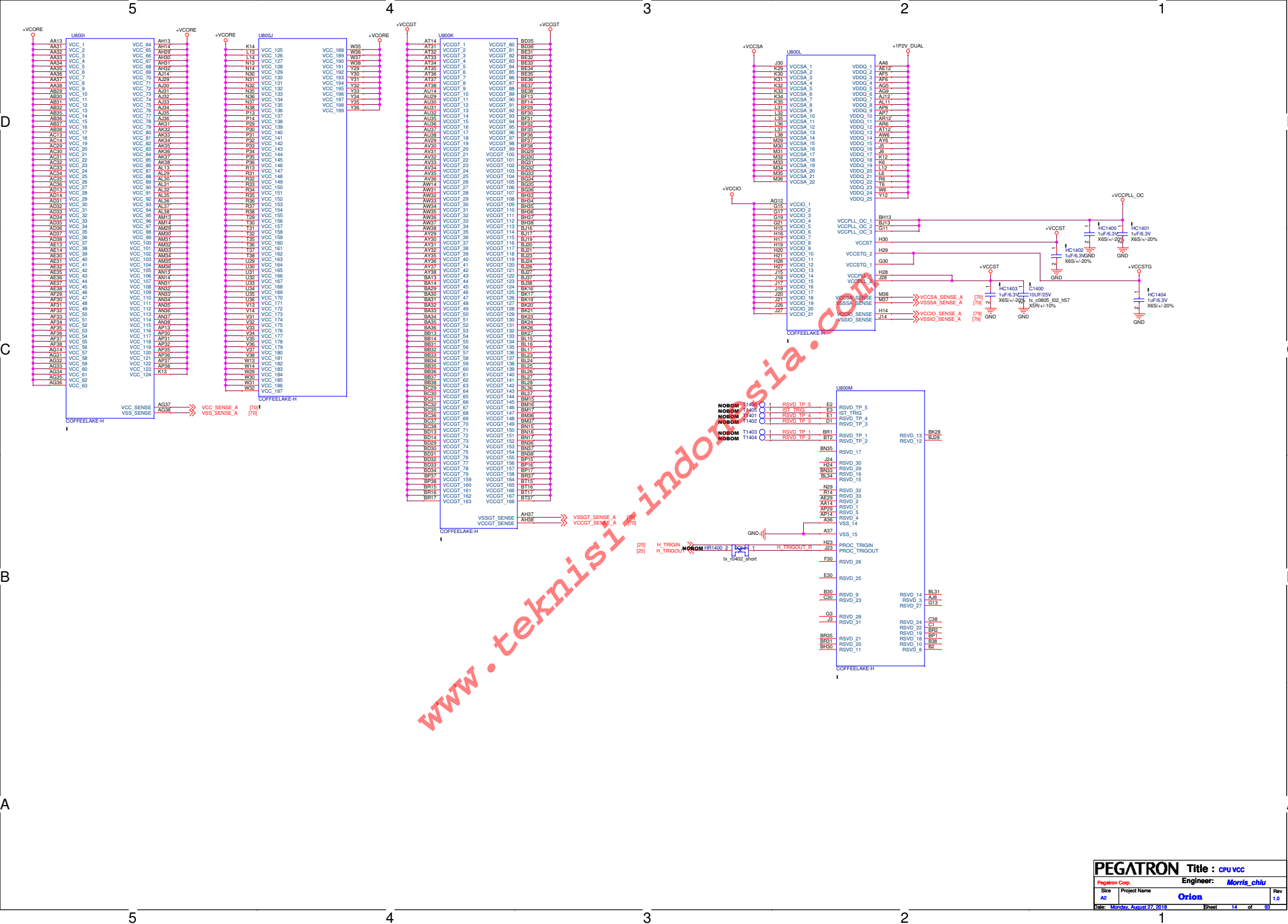
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BCUKP BCUKN	100 MHz Differential bus clock input to the processor	I		Diff	H and S-Processor Line
CLK24N CLK24P	24 MHz Differential bus clock input to the processor	I		Diff	
PCI_BCLKP PCI_BCLKN	100 MHz Clock for PCI Express* logic	I		Diff	



Signal Name	Description
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> • CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted: <ul style="list-style-type: none"> — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • CFG[1]: Reserved configuration lane. • CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. <ul style="list-style-type: none"> — 1 = Normal operation — 0 = Lane numbers reversed. • CFG[3]: Reserved configuration lane. • CFG[4]: eDP enable: <ul style="list-style-type: none"> — 1 = Disabled. — 0 = Enabled. • CFG[6:5]: PCI Express* Bifurcation <ul style="list-style-type: none"> — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • CFG[7]: PEG Training: <ul style="list-style-type: none"> — 1 = (default) PEG Train Immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • CFG[19:8]: Reserved configuration lanes.

Pin Name	Strap Description	Configuration (Default Value for Each Bit is 1 Unless Specified)	Default Value	✓
CFG[19:8]	Reserved configuration lands.			





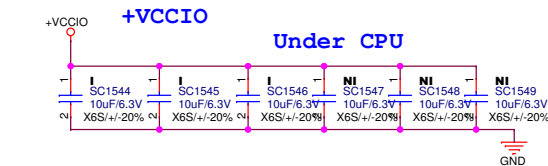
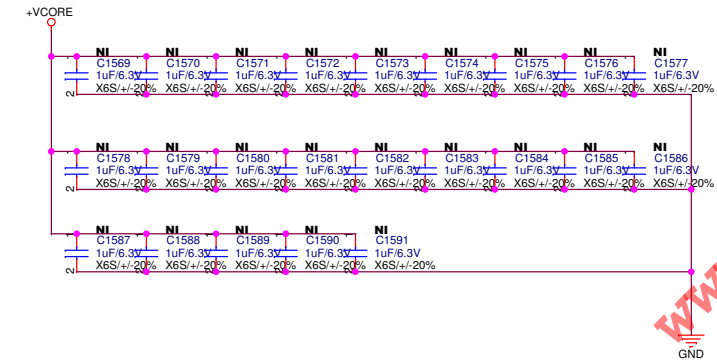
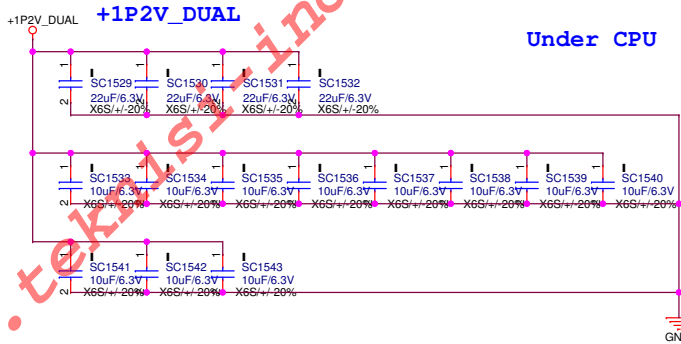
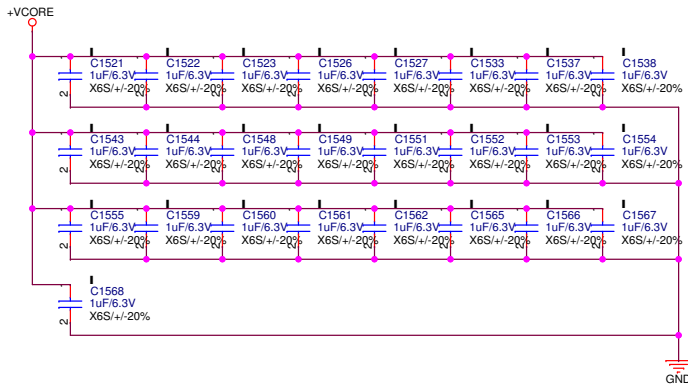
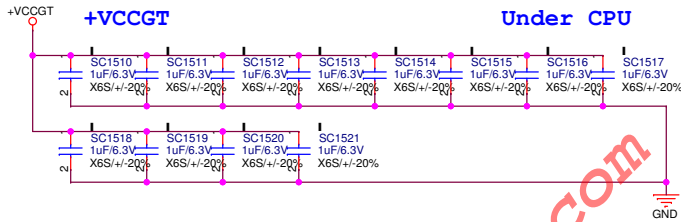
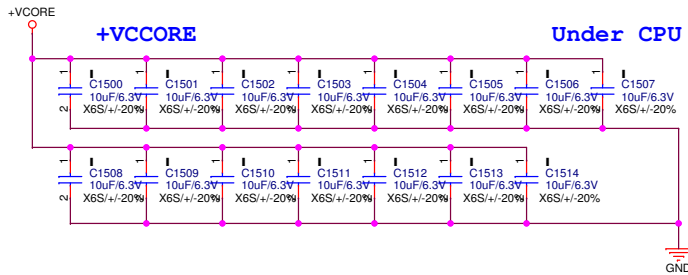
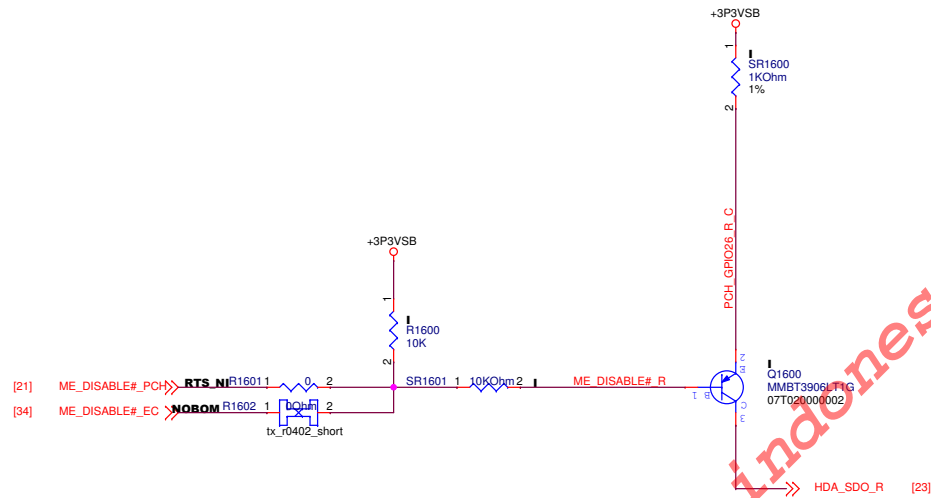


Table 50-3. Decoupling Requirements for CFL H Processor

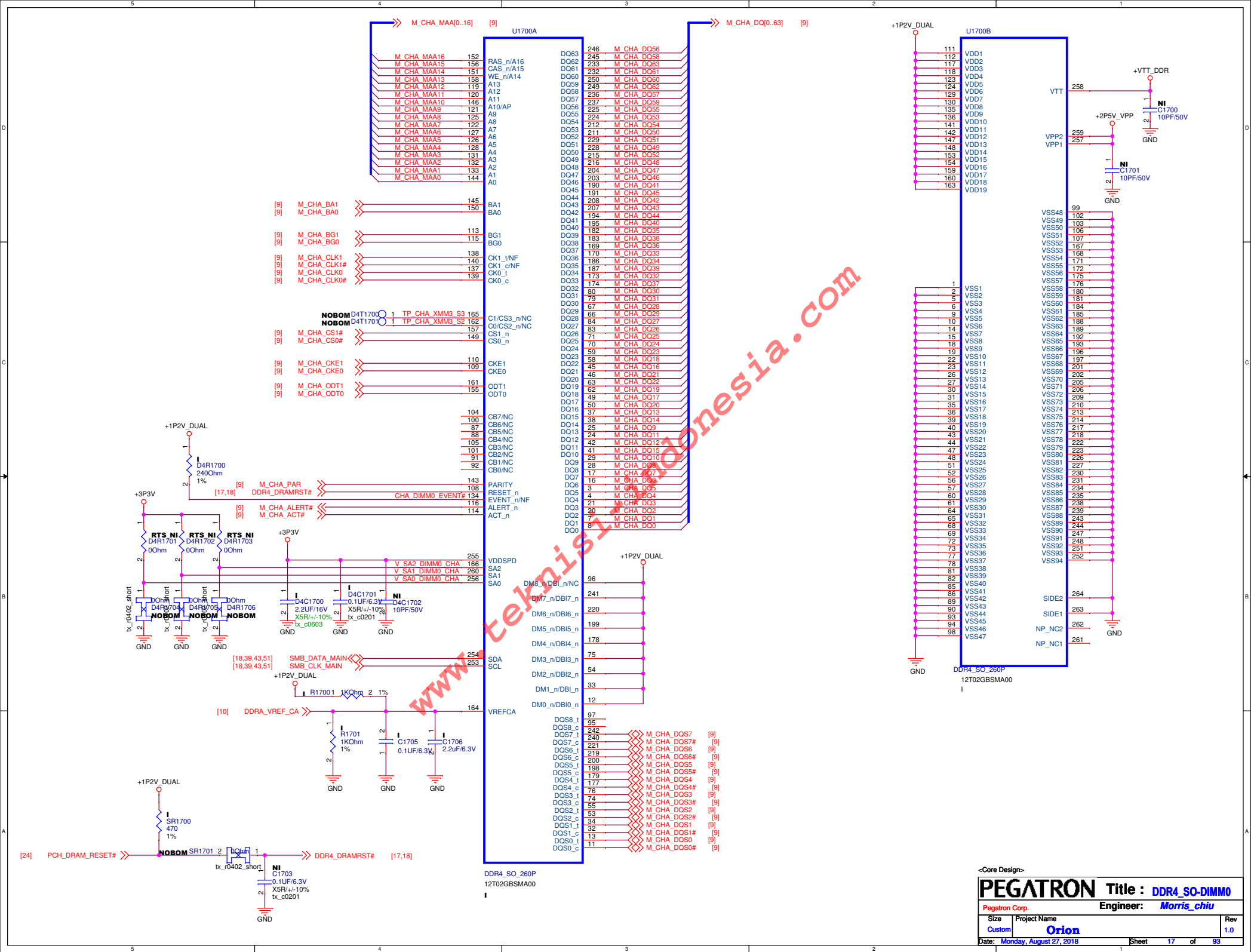
Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805	12x 22uF 0603	Place as close to the BGA as possible
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
VccGT	3x 47uF 0805 7x 22uF 0603	10x 10uF 0402	
		12x 1uF 0201	
VccSA	2x 47uF 0805 2x 22uF 0603	7x 10uF 0402	
		1x 1uF 0201	
VDDQ		4x 22uF 0603	
		11x 10uF 0402	
VccIO		3x 10uF 0402	Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate.
		3x 0402 (placeholder)	

ME Disable

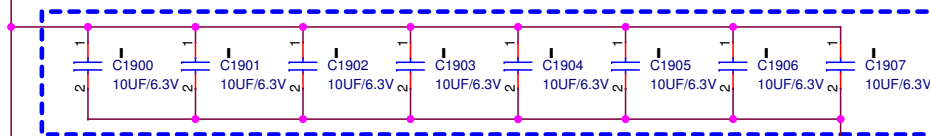


PEGATRON DT-MB RESTRICTED SECRET

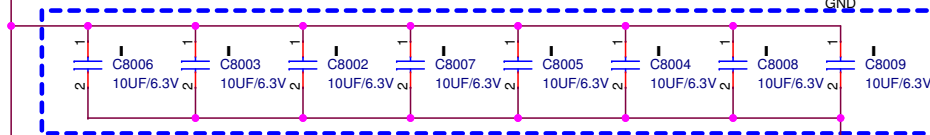
PEGATRON		Title : ME disable	
Pegatron Corp.		Engineer: Morris_chiu	
Size A3	Project Name Orion	Rev 1.0	
Date: Monday, August 27, 2018		Sheet 16 of 93	



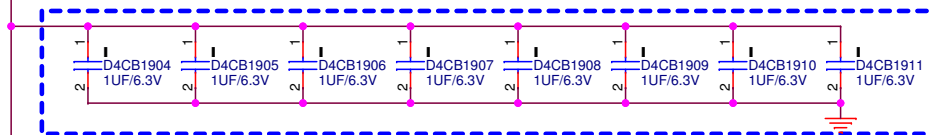
+1P2V_DUAL



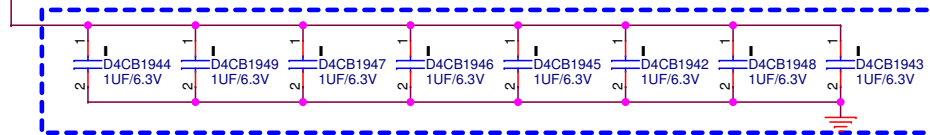
close
CH A SO-DIMM



close
CH B SO-DIMM



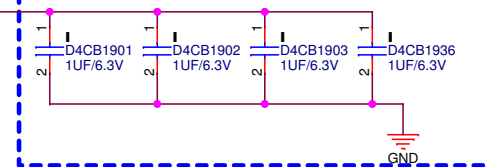
close
CH A SO-DIMM



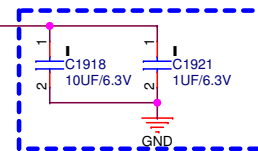
close
CH B SO-DIMM

+VTT_DDR

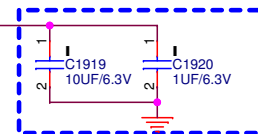
Near SO-DIMM



+2P5V_VPP



close CH A SO-DIMM



close CH B SO-DIMM

DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)	Note
DDR4 2 Channels SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10 μ F (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1 μ F (0402)	
		1 placeholder	1x 330 μ F (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10 μ F (0603)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10 μ F (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1 μ F (0402)	
	VPP	DRAM Side	2x 10 μ F (0603)	
		DRAM Side	2x 1 μ F (0402)	
	VDDSPD	Place close to DIMM	1x 0.1 μ F (0402)	
		Place close to DIMM	1x 2.2 μ F (0402)	

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : DDR4 DECOUPLING	
Pegatron Corp.		Engineer: Morris_chiu	
Size Custom	Project Name Orion	Rev 1.0	
Date: Monday, August 27, 2018		Sheet 19 of 93	

(LAN) Killer NIC

M.2 KEY-E WLAN

HDD

M.2 PCIE X4 #2

NOBOM T2103

NOBOM T2110

NOBOM T2102

NOBOM T2102

NOBOM T2102

NOBOM T2102

NOBOM T2102

NOBOM T2102

NOBOM T2102

NOBOM T2102

NOBOM T2102

NOBOM T2102

NOBOM T2102

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NOBOM T2102

NOBOM T2102

NOBOM T2102

NOBOM T2102

NOBOM T2102

NOBOM T2102

Version	Board ID. 1	Board ID. 2	Board ID. 3
B01	1	1	1
X00	0	1	1
X01	0	0	1
A00	0	0	0

NOTE:

GPP_J4

Pin Strap for XTAL frequency selection
An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 Mhz XTAL operation

NOTE:

GPP_J6 / CNV_RGI_DT / UART0_TXD

0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

NOTE:

GPP_J9 / CNV_MFUART2_TXD

The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail

PEGATRON Title : PCH SATA/PCIE

Size	Project Name	Engineer:	Rev
A2	Orion	Morris_chiu	1.0
Date: Monday, August 27, 2018		Sheet	21 of 93

NOTE:
eSPI operates at 1.8V

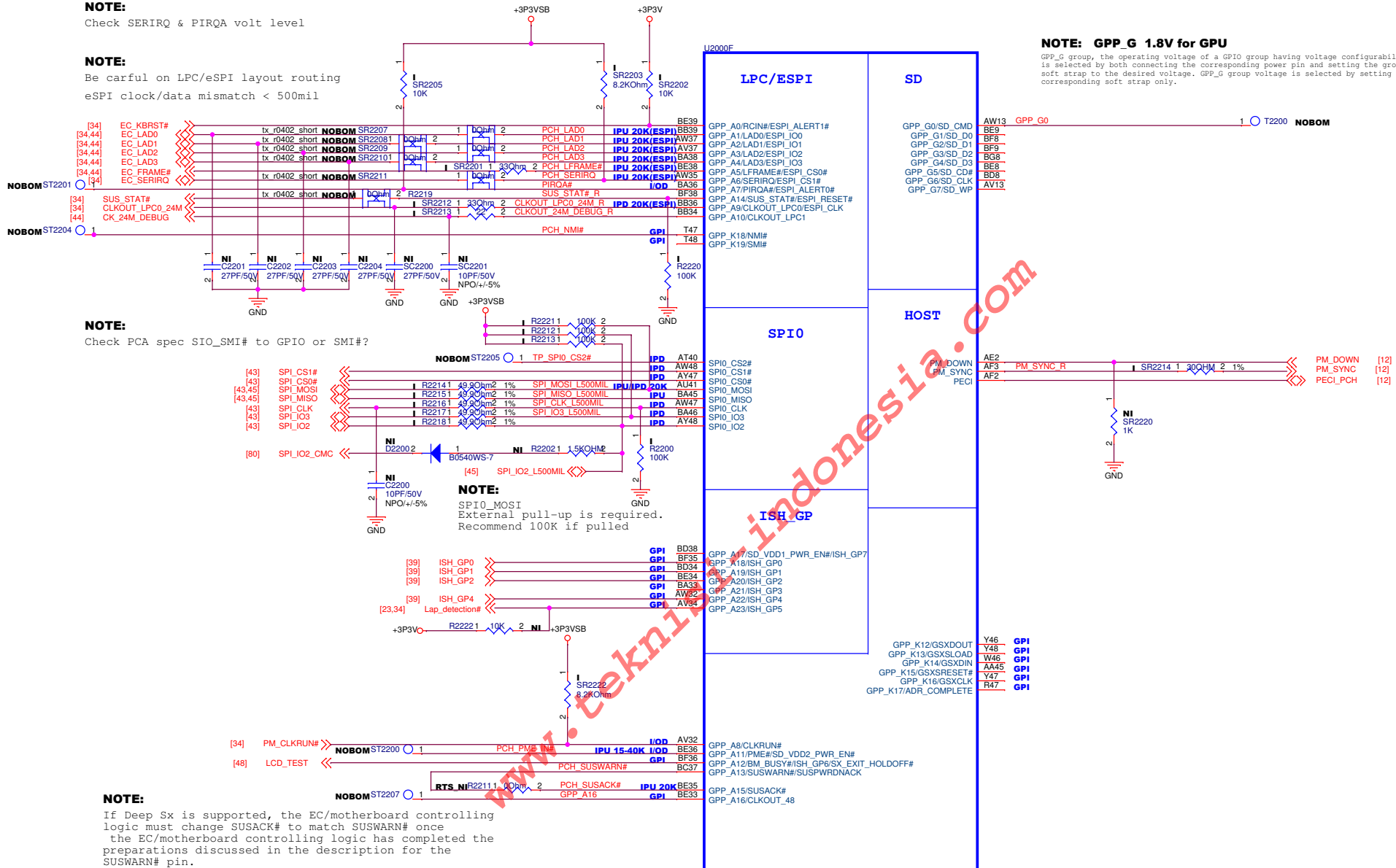
NOTE:
Check GPP_A0 power well

NOTE:
Check SERIRQ & PIRQA volt level

NOTE:
Be careful on LPC/eSPI layout routing
eSPI clock/data mismatch < 500mil

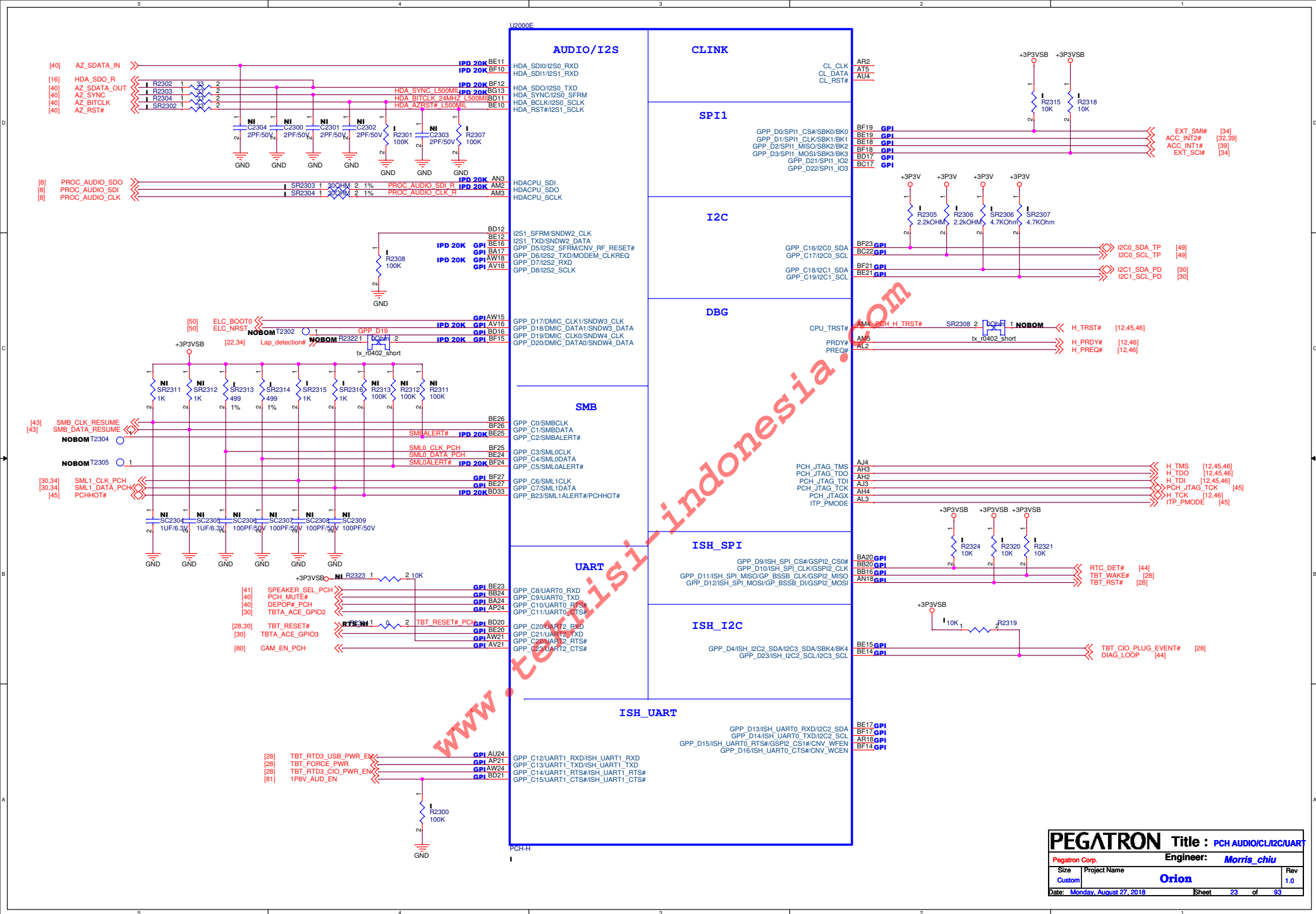
NOTE: GPP_G 1.8V for GPU

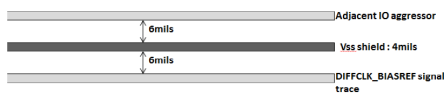
GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage selection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.



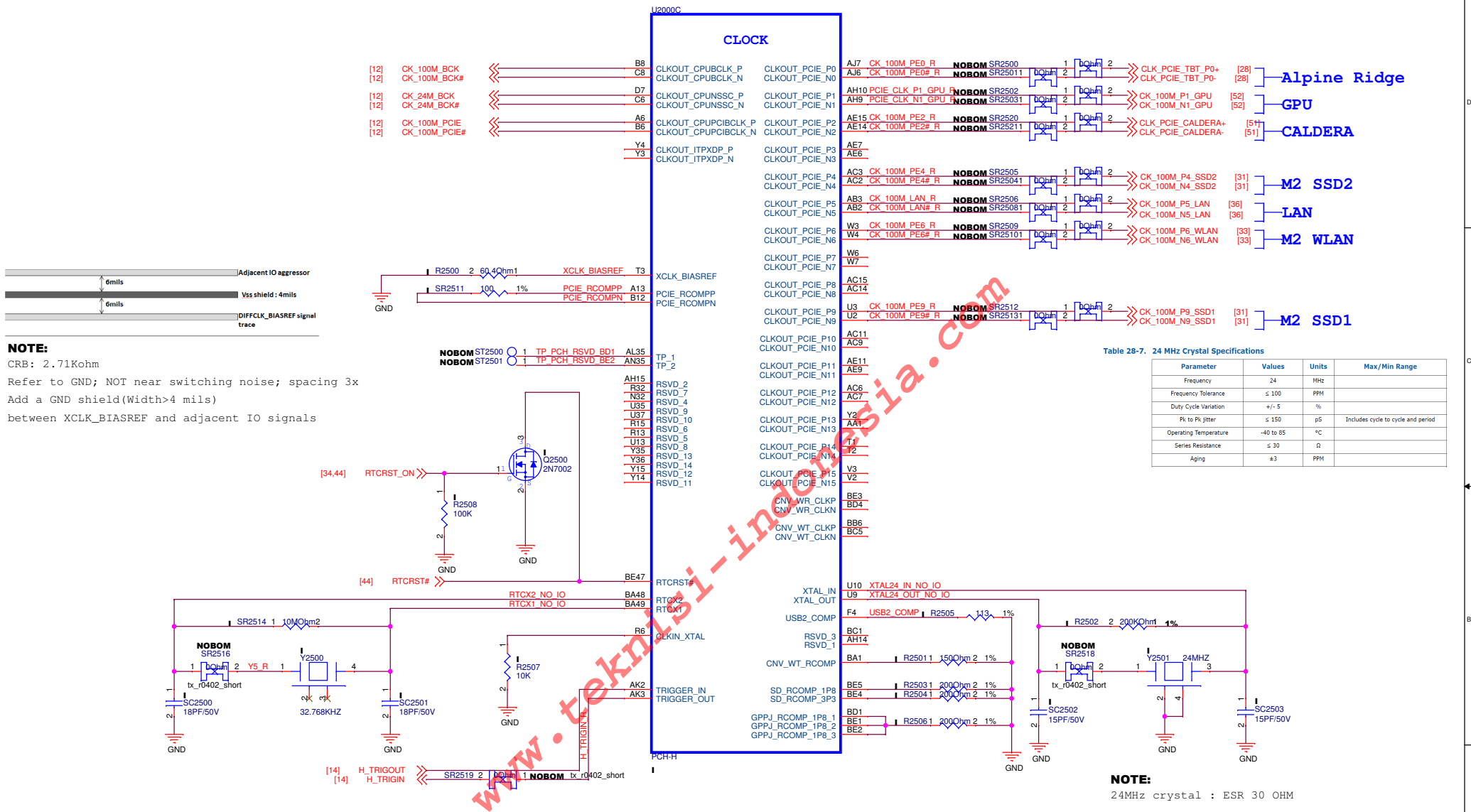
PEGATRON DT-MB RESTRICTED SECRET

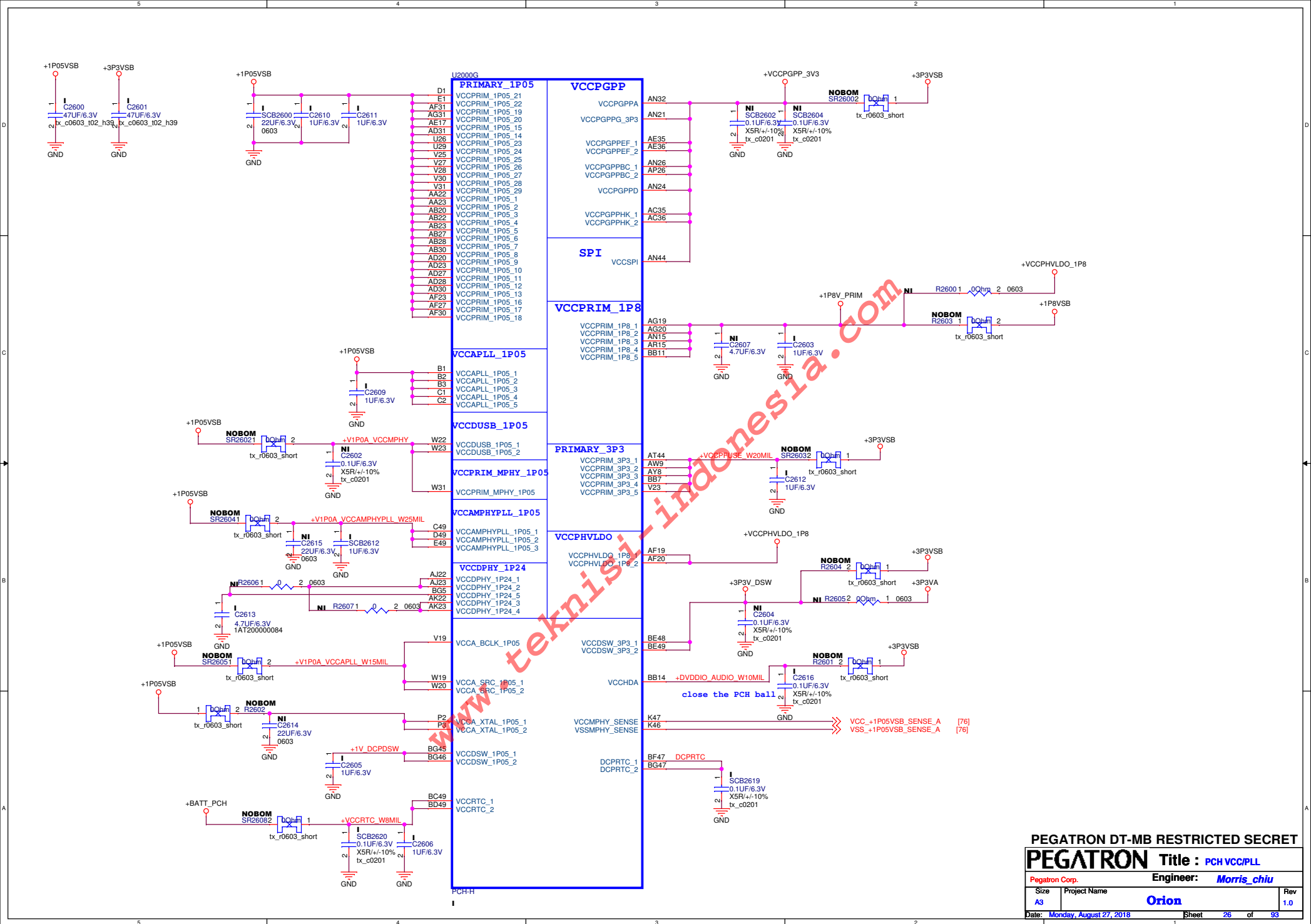
PEGATRON		Title : PCH ESPI/SPI/FAN/HOST	
Pegatron Corp.		Engineer: Morris_chiu	
Size Custom	Project Name Orion		Rev 1.0
Date: Monday, August 27, 2018		Sheet 22 of 93	

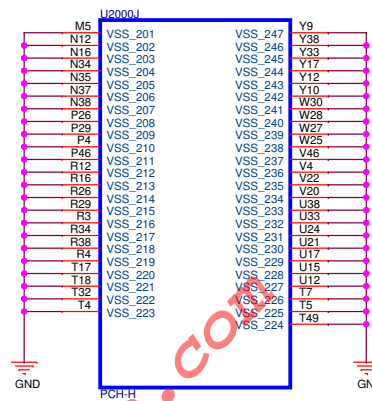
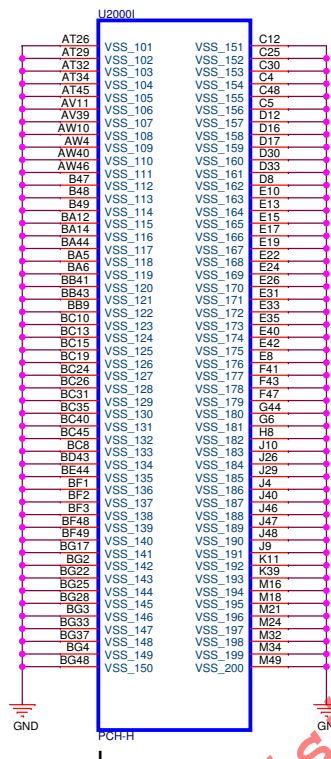
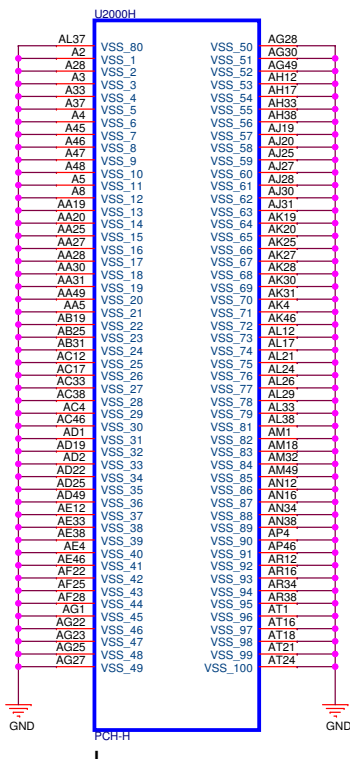


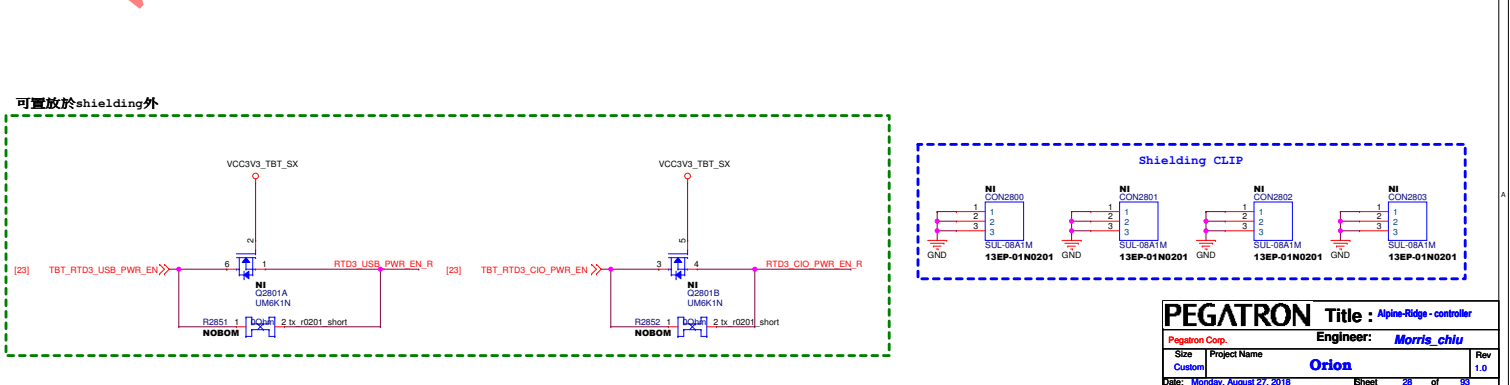
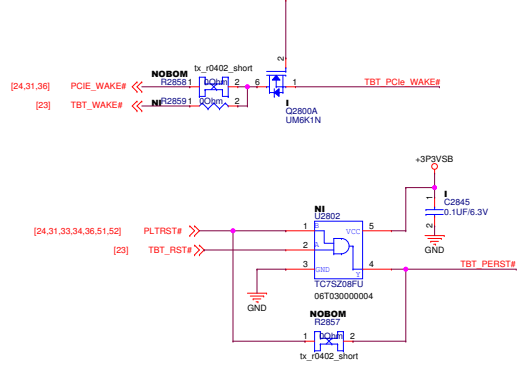
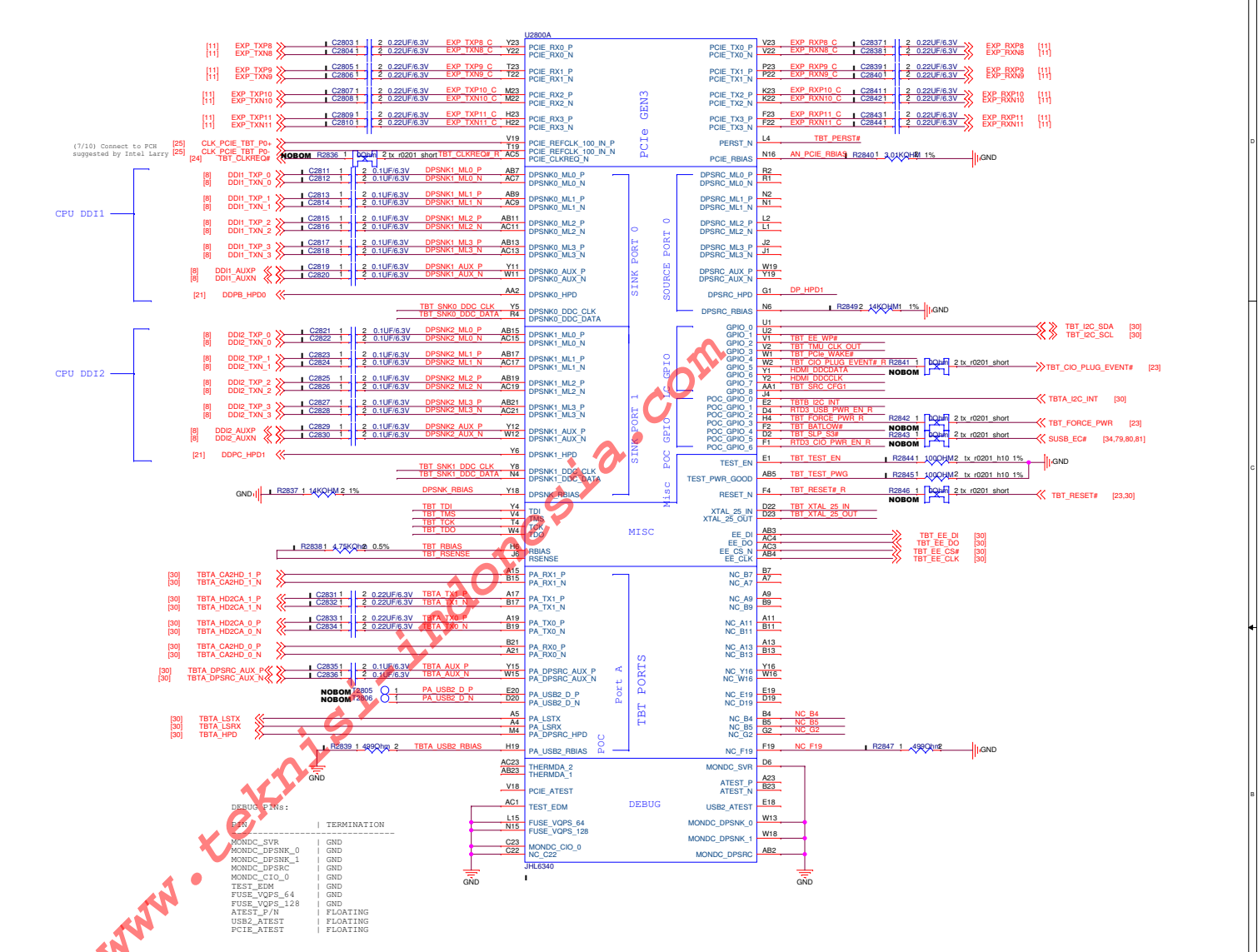
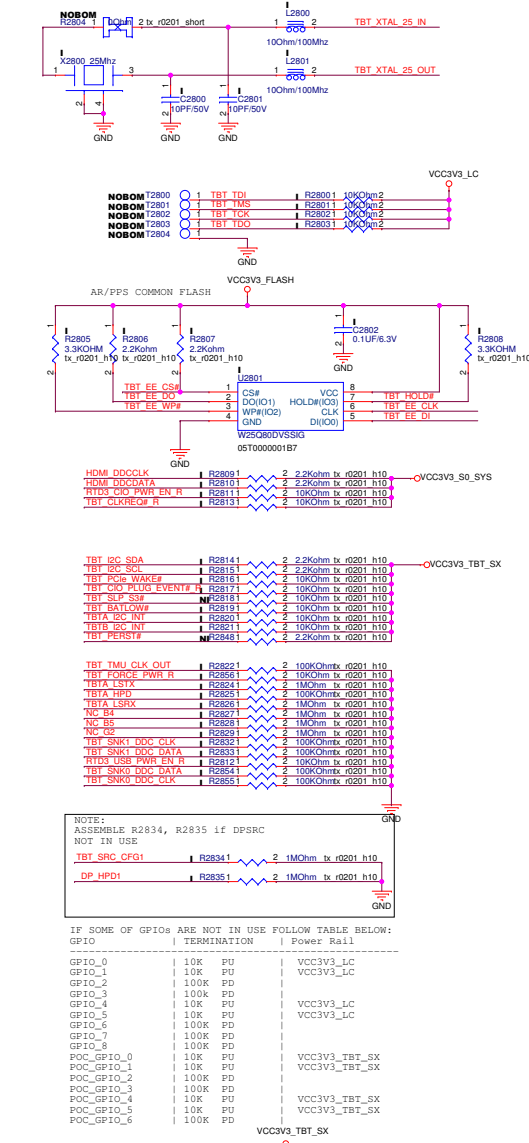


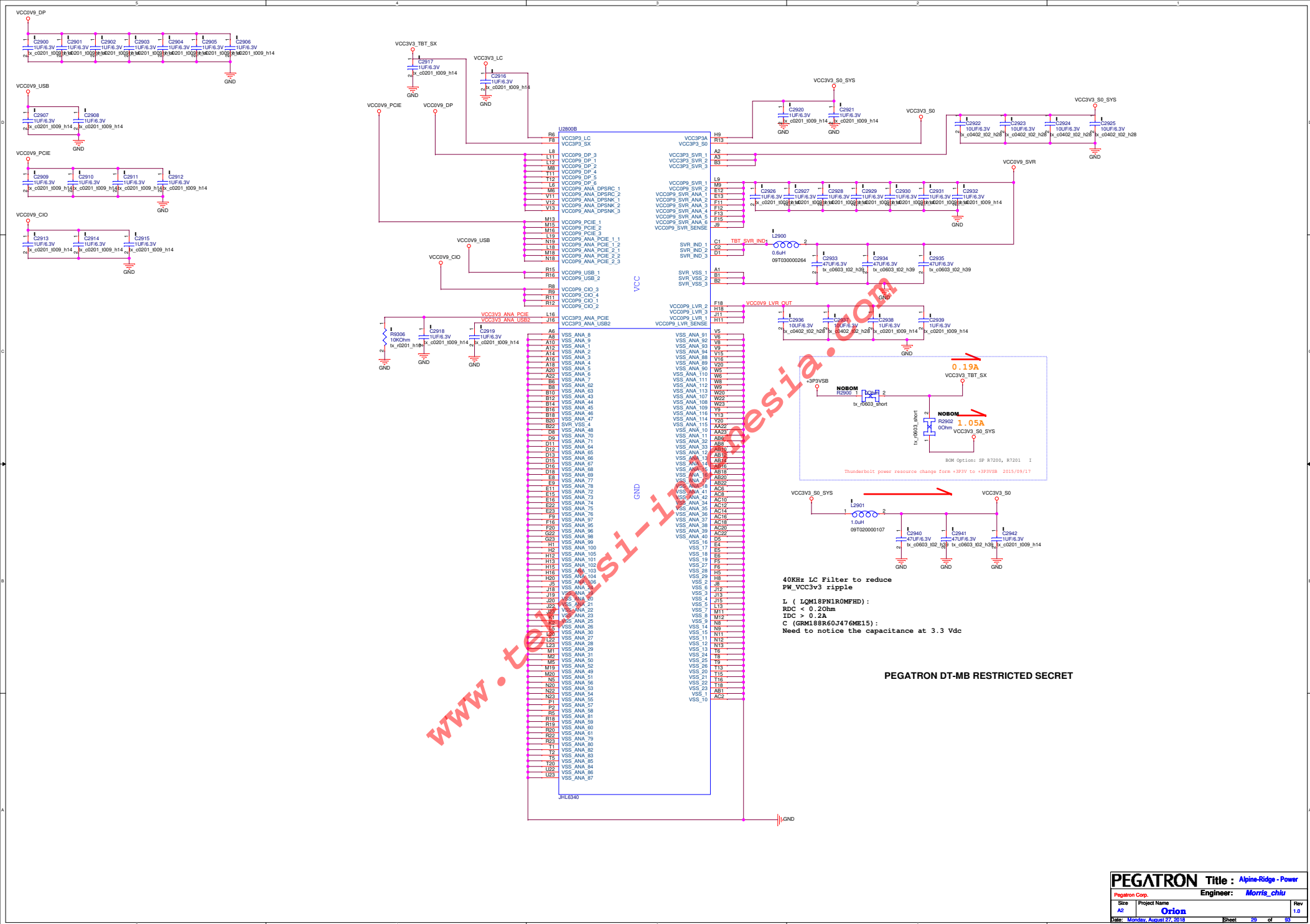
NOTE:
CRB: 2.71Kohm
Refer to GND; NOT near switching noise; spacing 3x
Add a GND shield(Width>4 mils)
between XCLK_BIASREF and adjacent IO signals

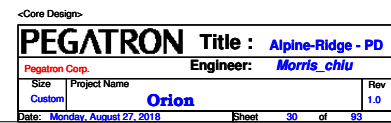




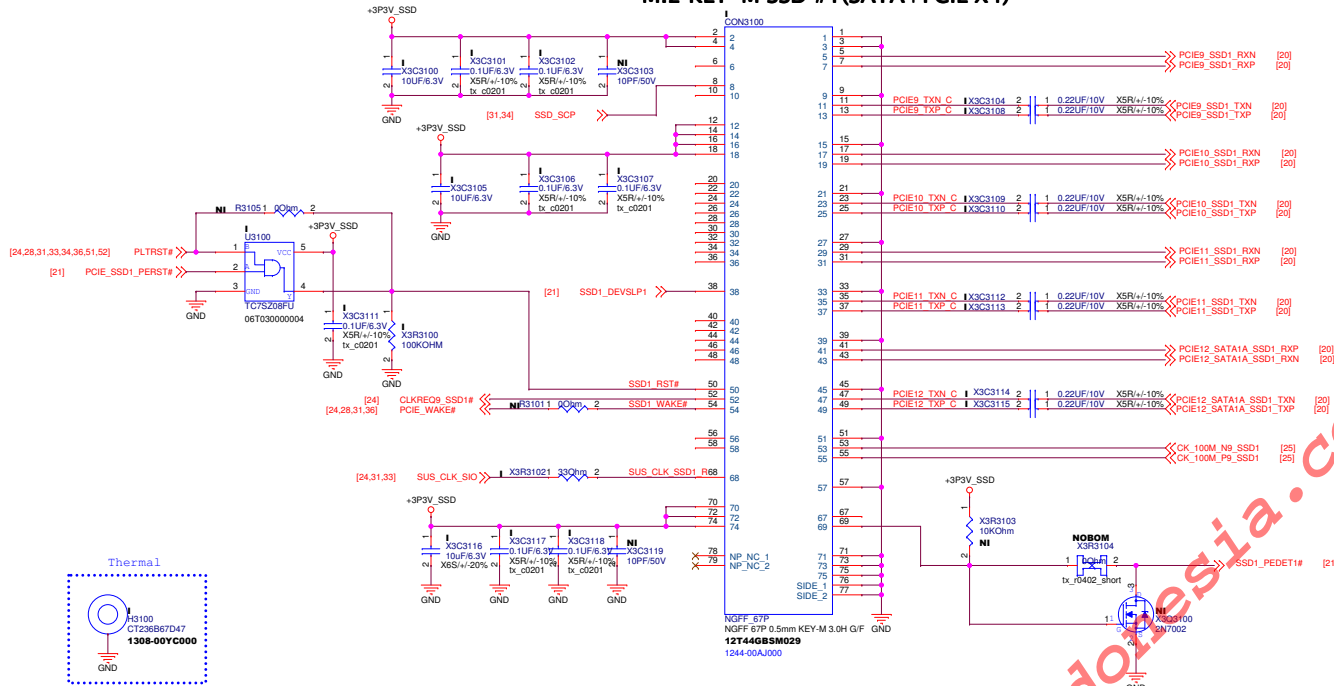




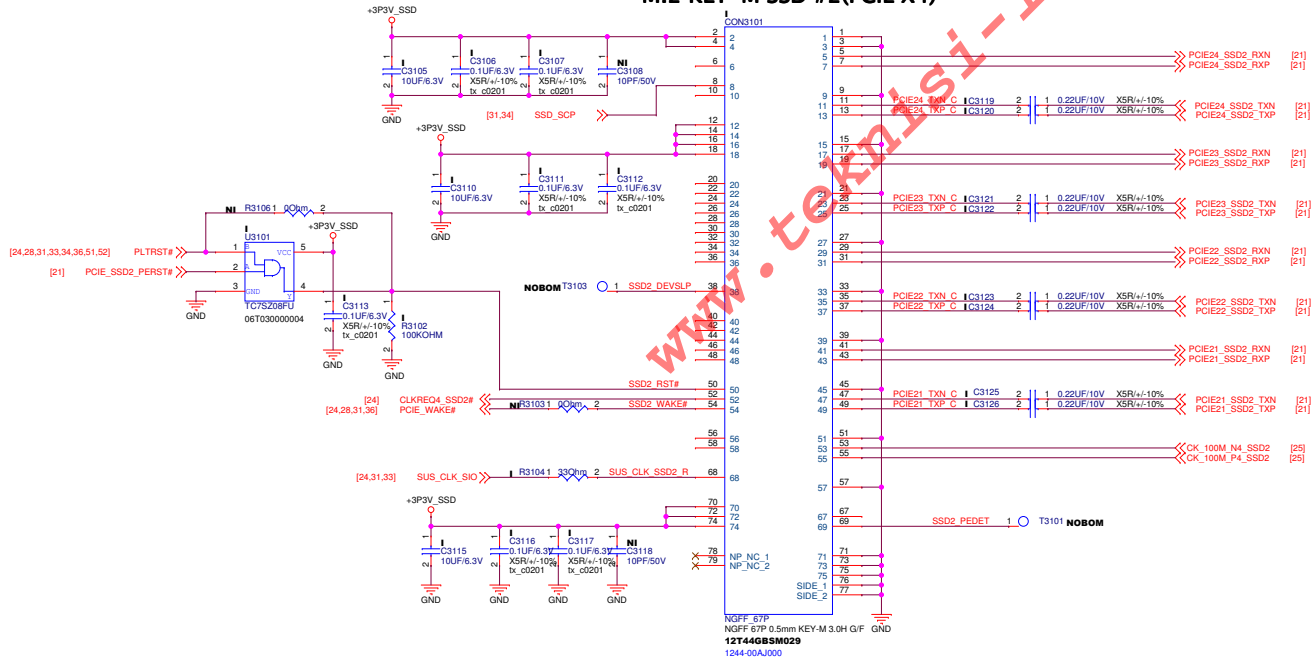


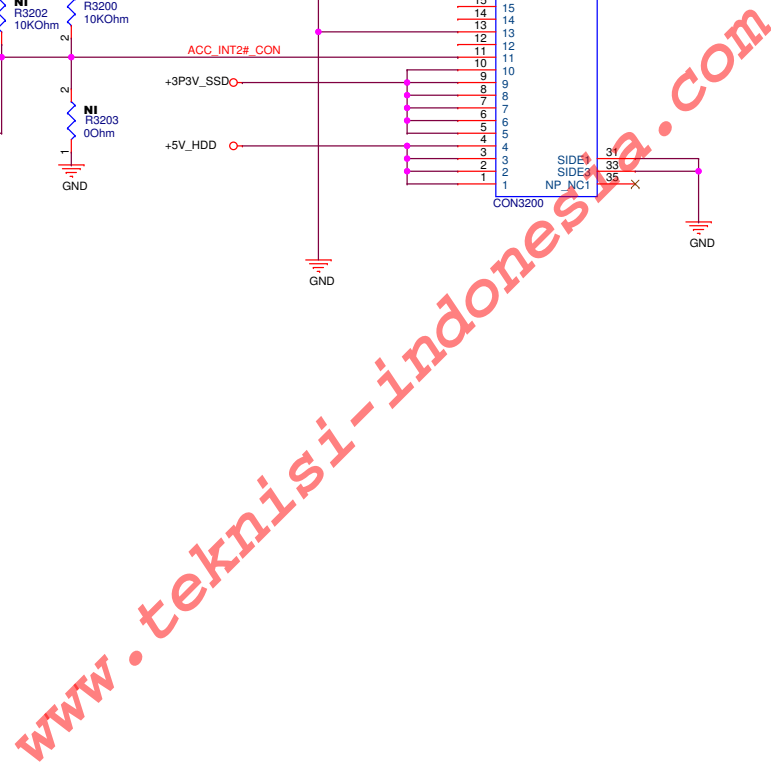


M.2 KEY-M SSD #1(SATA+PCIE X4)



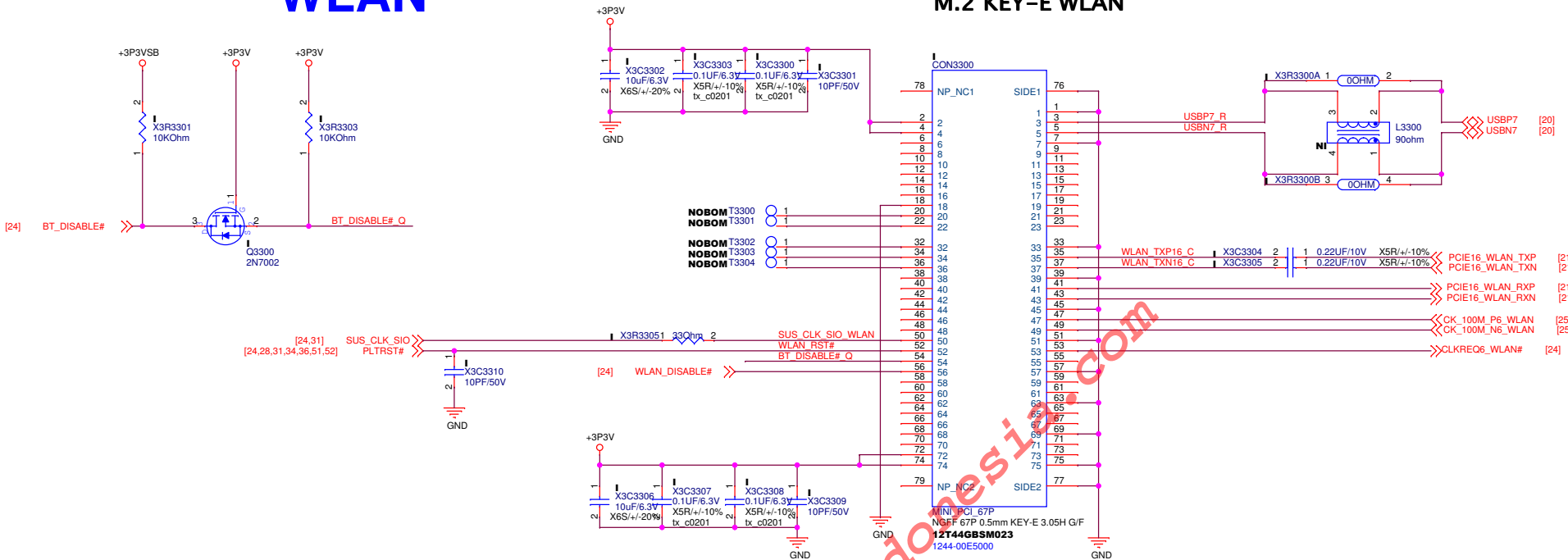
M.2 KEY-M SSD #2(PCIE X4)





PEGATRON		Title : <i>SATA HDD</i>	
Pegatron Corp.		Engineer: <i>Morris_chiu</i>	
Size <i>A3</i>	Project Name <i>Orion</i>	Rev <i>1.0</i>	
Date: <i>Monday, August 27, 2018</i>		Sheet	<i>32</i> of <i>93</i>

WLAN

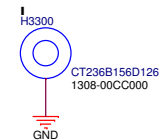
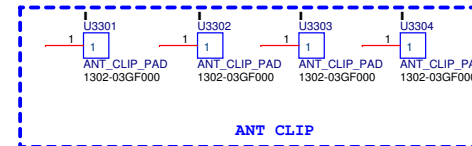


59	PERp1	NC	60	I2C_CLK[I]	NC
57	GND	YES	58	I2C_DATA[IO]	NC
55	PCIE_WAKE_L	YES	56	WLAN_DISABLE_L	YES
53	PCIE_CLKREQ_L	YES	54	BT_DISABLE_L	YES
51	GND	YES	52	PCIE_RST_L	YES
49	REFCLKNO	YES	50	SUSCLK(32kHz)	NC(Reverse resister)
47	REFCLKPO	YES	48	LTE_SYNC	YES
45	GND	YES	46	LTE_PRI	YES
43	PETn0	YES	44	LTE_ACTIVE	YES
41	PETp0	YES	42	RSVD	NC
39	GND	YES	40	RSVD	NC
37	PERn0	PCIE_TX_P	38	RSVD	NC
35	PERp0	PCIE_TX_N	36	UART_CTS	YES
33	GND	YES	34	UART_RTS	YES
31	NC	NC	32	UART_RXD	YES
29	NC	NC	30	NC	NC
27	NC	NC	28	NC	NC
25	NC	NC	26	NC	NC
23	NC	NC	24	NC	NC
21	NC	NC	22	UART_TXD	YES
19	DBG_UART_RXD	YES	20	UART_WAKEHOST_L	YES
17	DBG_UART_TXD	YES	18	GND	YES
15	NC	NC	16	LED_BT	YES
13	NC	NC	14	NC	NC
11	NC	NC	12	NC	NC
9	NC	NC	10	NC	NC
7	GND	YES	8	NC	NC
5	USB_D_N	YES	6	LED_WLAN	YES
3	USB_D_P	YES	4	3.3V	YES
1	GND	YES	2	3.3V	YES

M.2 KEY-E WLAN

Pin #	Name	DUT Connection	Pin #	Name	DUT Connection
75	GND	YES	74	3_3V	YES
73	REFCLKN1	NC	72	3_3V	YES
71	REFCLKP1	NC	70	PEWAKE1	NC
69	GND	YES	68	CLKREQ1	NC
67	PETn1	NC	66	PERST1	NC
65	PETp1	NC	64	RSVD	NC(Reverse resister)
63	GND	YES	62	ALERT[0]	NC
61	PERn1	NC			

Remark: 1. NC is not connected; YES is connected.
 2. Pin54 is BT_DISABLE_L; Pin56 is WLAN_DISABLE_L.
 3. Pin 20,22,32,34 and 36 are GPIO and have internal pull up(QCA6174A75), Suggest platform NC those pins.
 4. Pin44, 46, 48, QCA suggest platform to NC.
 5. Pin17 and 19 suggest reserve test point at platform side.



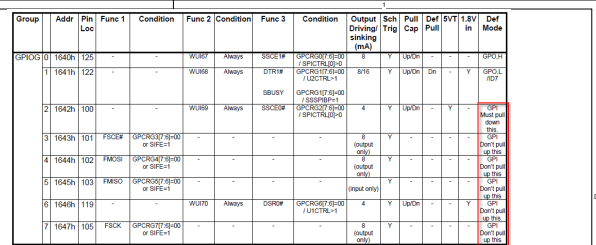
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : M.2 KEY-A 2230 WLAN

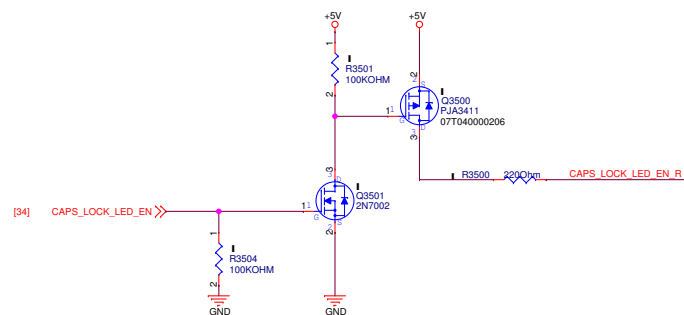
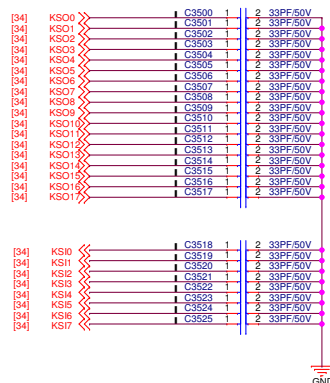
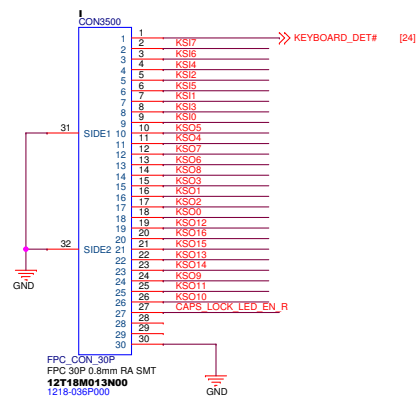
Pegatron Corp. Engineer: Morris_chiu

Size A3 Project Name Orion Rev 1.0

Date: Monday, August 27, 2018 Sheet 33 of 93

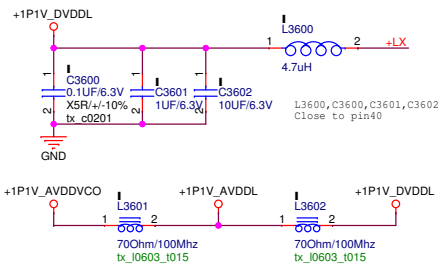
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KeyBoard connector

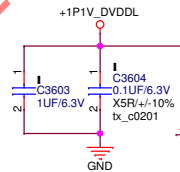
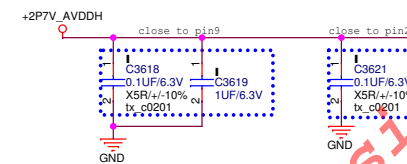
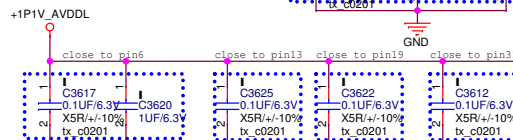
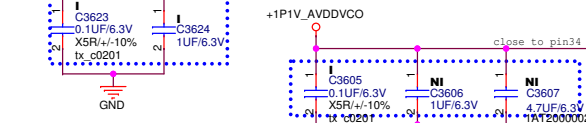
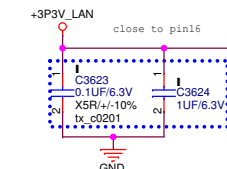
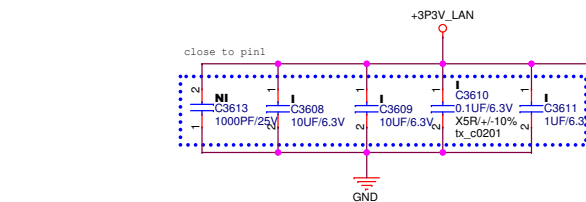


1 C3518 1 2 33PF.50V
 1 C3519 1 2 33PF.50V
 1 C3520 1 2 33PF.50V
 1 C3521 1 2 33PF.50V
 1 C3522 1 2 33PF.50V
 1 C3523 1 2 33PF.50V
 1 C3524 1 2 33PF.50V
 1 C3525 1 2 33PF.50V

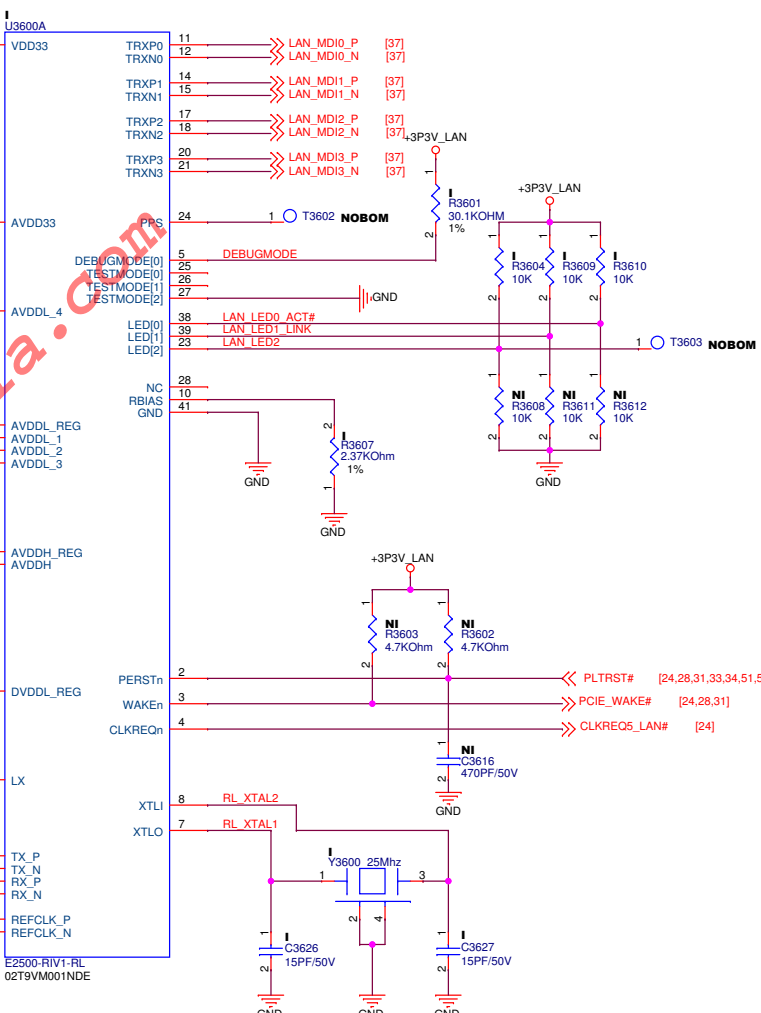
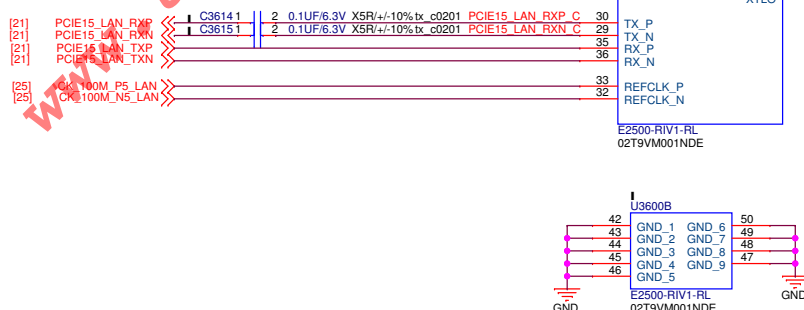
GND



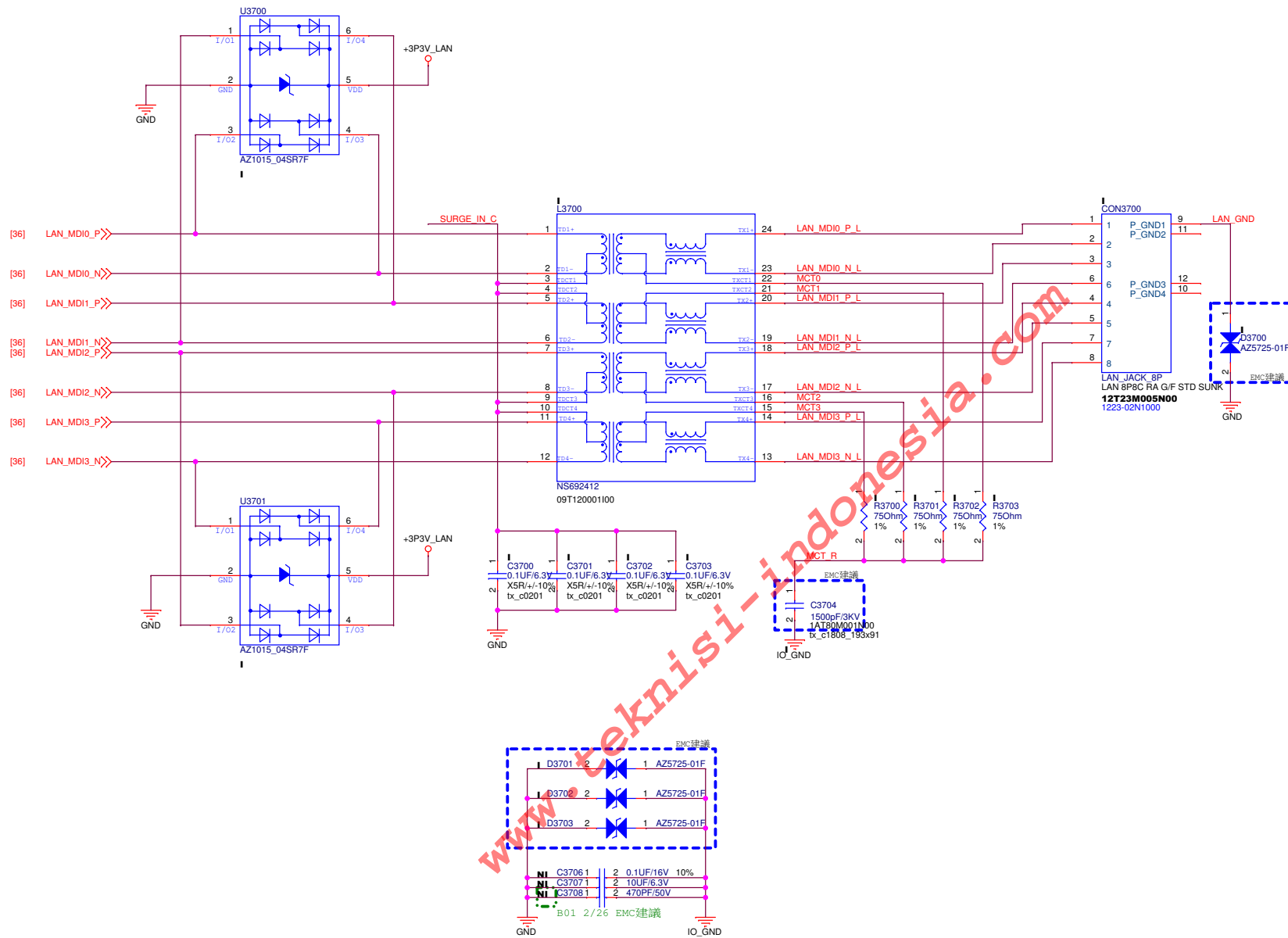
**If AVDDL/DVDDL comes from internal SWR: mount L3602;
If AVDDL/DVDDL comes from internal LDO: no mount L3602, L3600, C3600, C3601, C3602



U3600 & U3601 Co-lay
QCA8171-BL3A-R
02T3TM003NDE



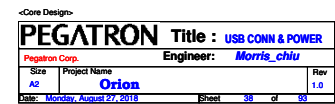
PEGATRON Title : LAN NIC KILLER			
Pegatron Corp.		Engineer: Morris_chiu	
Size	Project Name	Orion	Rev
A3			1.0
Date: Monday, August 27, 2018		Sheet 36 of 93	



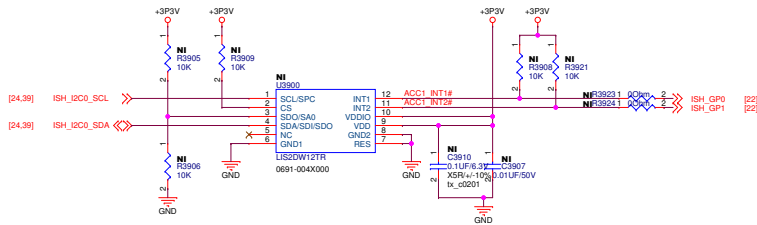
<Core Design>			
PEGATRON		Title : LAN JACK	
Pegatron Corp.		Engineer: Morris_chiu	
Size A3	Project Name Orion		Rev 1.0
Date: Monday, August 27, 2018		Sheet 37 of 93	

CTL1	CTL2	CTL3	ILIM_SEL	MODE	CURRENT LIMIT SETTING	STATUS OUTPUT (Active low)	COMMENT
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	
0	0	1	1	DCP_Auto	I_{LIM_HI} & ILIM_HI(1)	DCP load present(2)	Data Lines Disconnected
0	1	0	0	SDP1	ILIM_LO	OFF	Data Lines Disconnected and Load Detect Function Active
0	1	0	1	SDP1	ILIM_HI	OFF	Data Lines connected
0	1	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP load present(3)	Data Lines Disconnected and Load Detect Function Active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device Forced to stay in DCP BC1.2 charging mode
1	0	1	0	DCP / Divider1	ILIM_LO	OFF	Device Forced to stay in DCP Divider1 Charging Mode
1	0	1	1	DCP / Divider1	ILIM_HI	OFF	
1	1	0	0	SDP1	ILIM_LO	OFF	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	OFF	
1	1	1	0	SDP2(4)	ILIM_LO	OFF	
1	1	1	1	DCP(4)	ILIM_HI	DCP load present(5)	Data Lines Connected and Load Detect Active

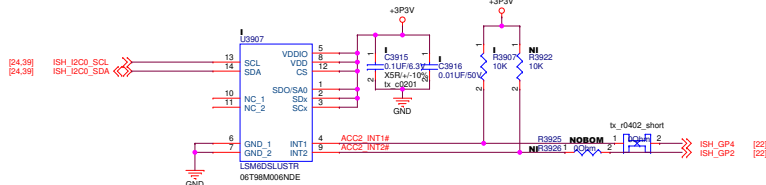
-
- The diagram illustrates a USB to RS485 converter module. The top section shows the USB interface with pins for D+, D-, GND, and VBUS, connected to a USB3800 chip. The bottom section shows the RS485 interface with pins for A, B, and GND, connected to an RS485 driver chip. The module includes a 5V regulator, a USB to UART bridge, and a 1-wire interface.



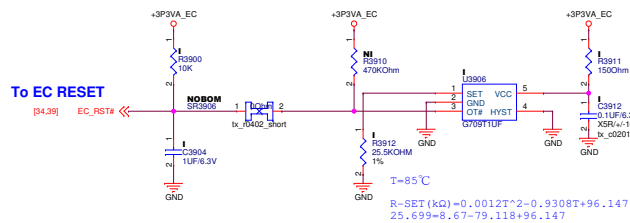
3-axis accelerometer



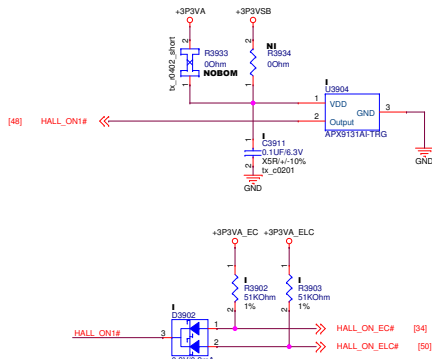
3D accelerometer and 3D gyroscope



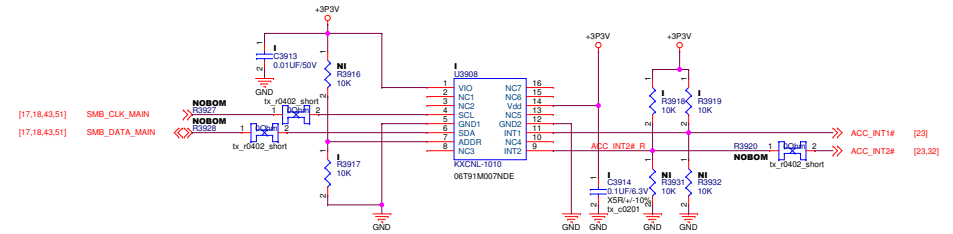
FOR HW thermal protection



HALL SENSOR

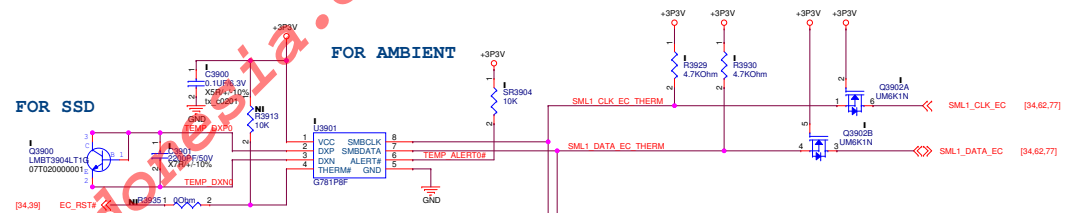


Free fall sensor

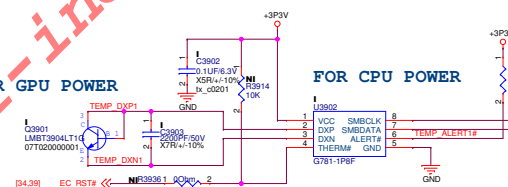


ADDR pin status	SAD	SAD + Read	SAD + Write
ADDR = 0	0011110 (1Eh)	00111101 (3Dh)	00111100 (3Ch)
ADDR = 1	0011101 (1Dh)	00111011 (3Bh)	00111010 (3Ah)

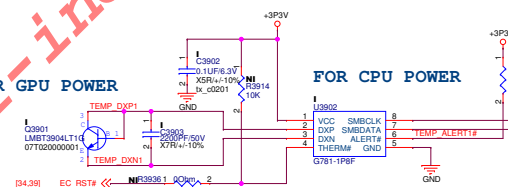
FOR SSD



FOR GPU POWER



FOR CPU POWER

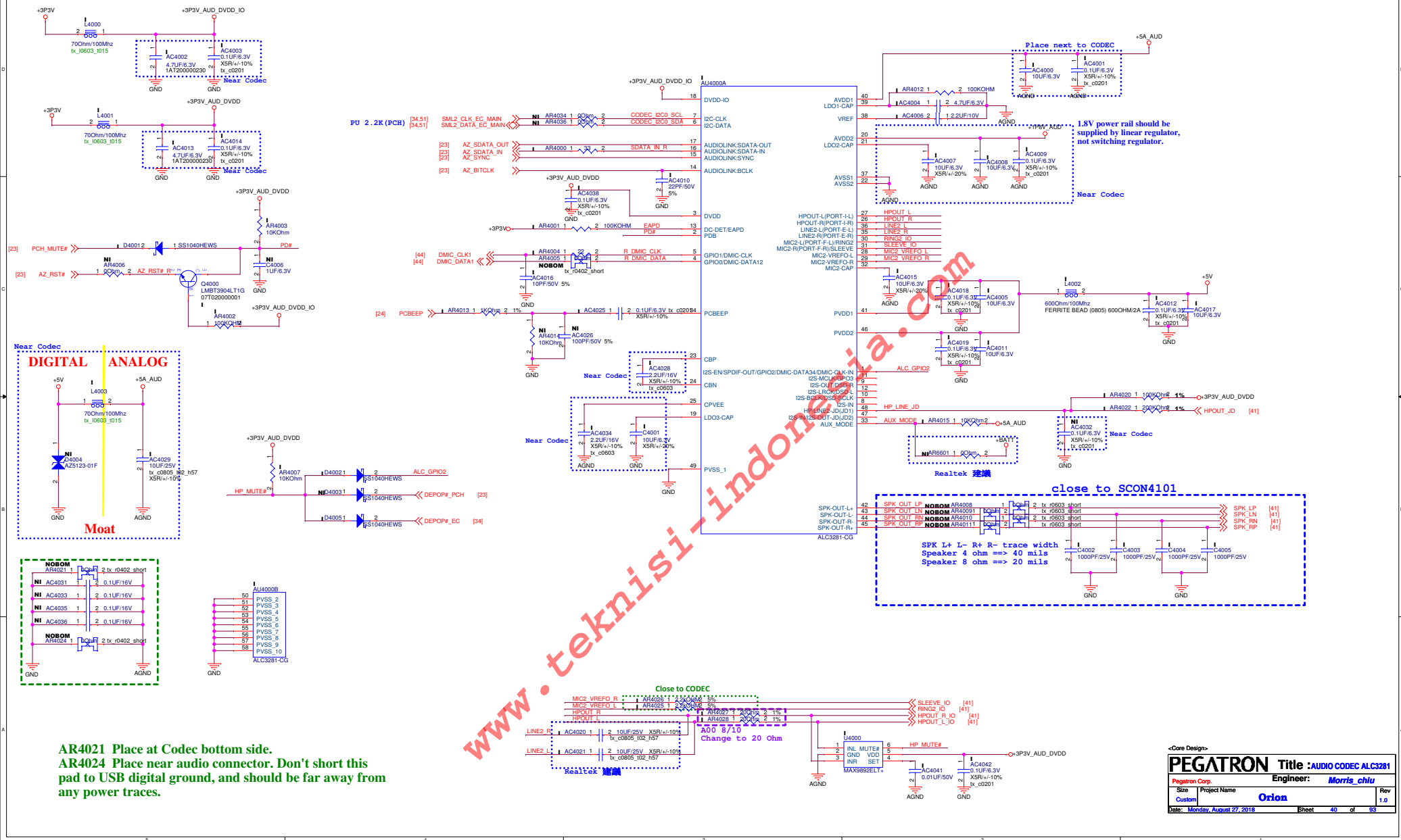


	A6	A5	A4	A3	A2	A1	A0
G781	1	0	0	1	1	0	0
G781-1	1	0	0	1	1	0	1

<Core Design>

PEGATRON Title : SENSOR			
Pegatron Corp		Engineer: Morris_chiu	
Size	Project Name	Orion	Rev
A2			1.0
Date: Monday, August 27, 2018		Sheet 39 of 39	

AUDIO CODEC- ALC3281

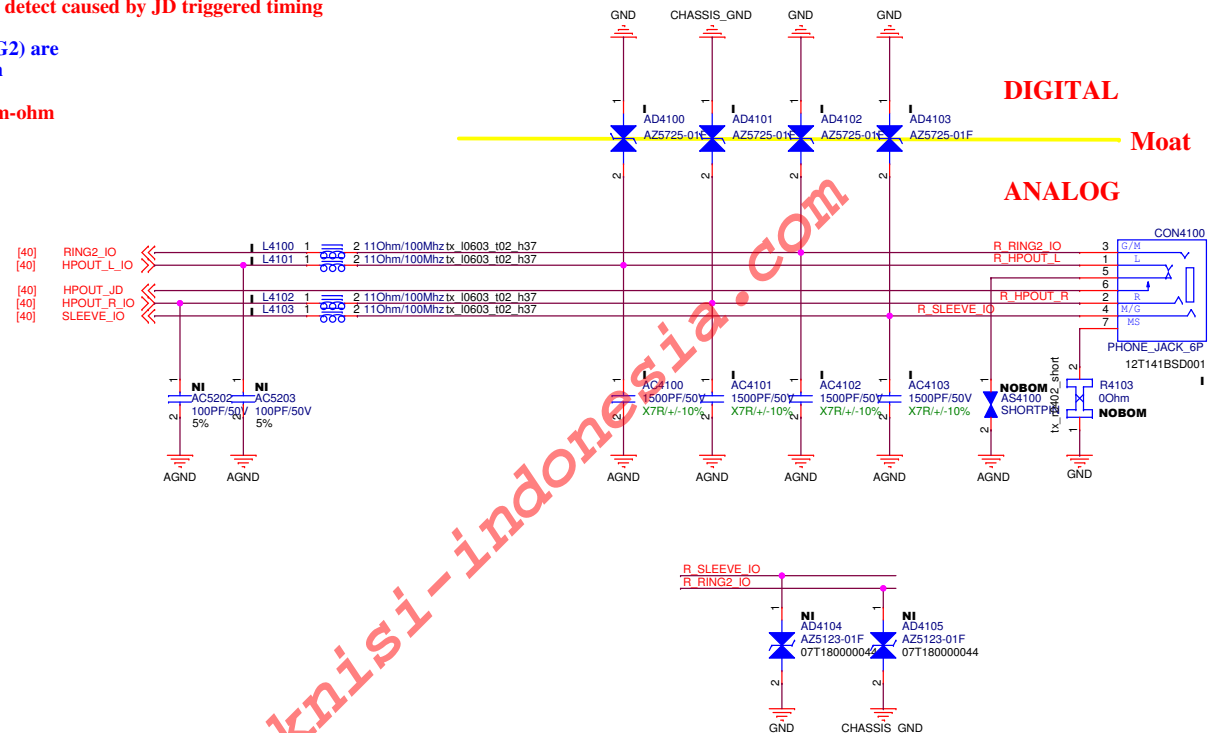


GLOBAL HEADSET CONNECTOR

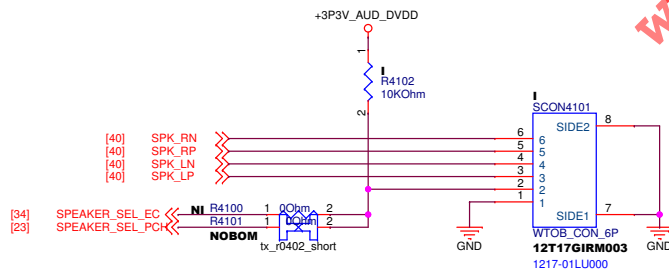
OMTP/CTIA headset, Headphone, Line-Out,
Microphone input, Line input.

This recommended phone-jack has moved #5/#6 Jack detect pin to the last position and lined up with #1 Tip pin.
This kind of design will significantly improve the false detect caused by JD triggered timing

PCB trace width of MIC2-R(SLEEVE)/MIC2-L(RING2) are
required at least 40 mil for HP crosstalk consideration
and, its length should be as short as possible.
L4100/L4103 should choose DC resistance (Rdc) < 30m-ohm
to get the best audio performance for HP crosstalk.



SPEAKER CONN



	15" FG	15" Zylux	17" FG	17" VECO	BIOS/EE setting
1st source (Pin1 & 2 open)	V		V		Pull High
2nd source (Pin1 & 2 short)		V		V	Pull Low

<Core Design>

PEGATRON Title : AUDIO JACK

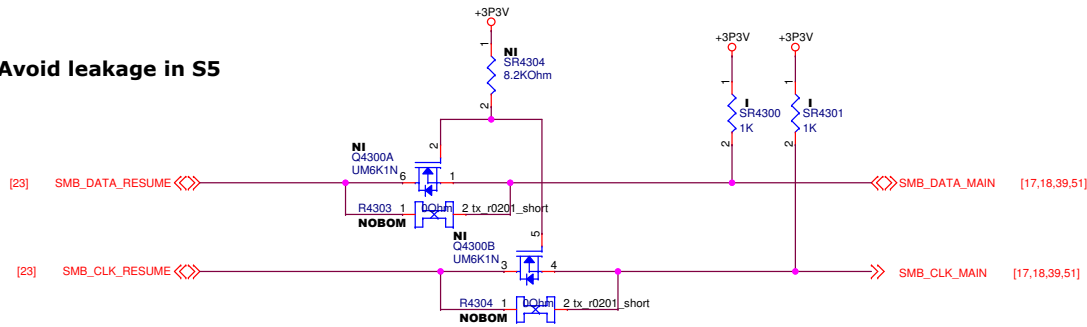
Pegatron Corp. Engineer: Morris_chiu
Size A3 Project Name Orion
Date: Monday, August 27, 2018 Sheet 41 of 93

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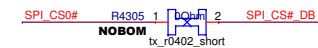
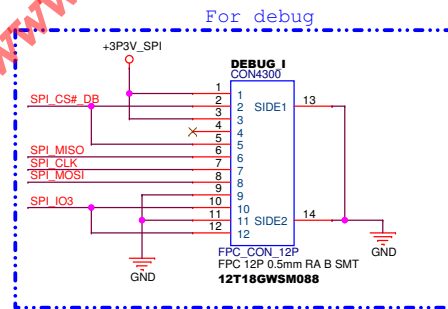
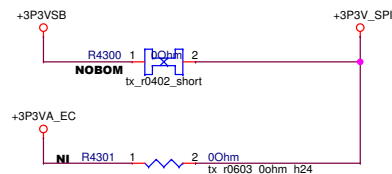
<Core Design>

PEGATRON		Title : USB Redriver	
Pegatron Corp.		Engineer: <i>Morris_chiu</i>	
Size	Project Name		Rev
A3	Orion		1.0
Date: <i>Monday, August 27, 2018</i>		Sheet <i>42</i> of <i>93</i>	

Avoid leakage in S5



SPI ROM (Quad I/O Supported)



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **SM BUS & SPI ROM**

Pegatron Corp. Engineer: **Morris_chiu**

Size A3 Project Name **Orion** Rev 1.0

Date: Monday, August 27, 2016 Sheet 43 of 93

[illegible]

CPU FAN CONNECTOR

The diagram illustrates the CPU Fan Connector circuit. It shows three +3.3V power inputs, each with a 4.7kOhm resistor (FB409, FB4403, FB4401). The circuit includes a 5V FAN and a 12V FAN. It features a 100PF/50V capacitor (FB4405) and a 100PF/50V capacitor (FB4404). The output is connected to a 12V FAN and a 5V FAN. The circuit is powered by a 3.3V input and a 5V input. The output is connected to a 12V FAN and a 5V FAN. The circuit is powered by a 3.3V input and a 5V input. The output is connected to a 12V FAN and a 5V FAN.

LPC DEBUG PORT

EC_LAD0 [22:34] ↔
 EC_LAD1 [22:34] ↔
 EC_LAD2 [22:34] ↔
 EC_LAD3 [22:34] ↔
 EC_FRAME# [22:34] ↔
 CK_X4M_DEBUG [22] ↔

DEBUG 1
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 2
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 3
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 4
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 5
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 6
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 7
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 8
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 9
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 10
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 11
 LCN4400

12
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 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 12
 LCN4400

12
 11
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 4
 3
 2
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DEBUG 13
 LCN4400

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DEBUG 14
 LCN4400

12
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 2
 1

DEBUG 15
 LCN4400

12
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 9
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 1

DEBUG 16
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 17
 LCN4400

12
 11
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 8
 7
 6
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 4
 3
 2
 1

DEBUG 18
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 19
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 20
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
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 2
 1

DEBUG 21
 LCN4400

12
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 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 22
 LCN4400

12
 11
 10
 9
 8
 7
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 4
 3
 2
 1

DEBUG 23
 LCN4400

12
 11
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 9
 8
 7
 6
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 4
 3
 2
 1

DEBUG 24
 LCN4400

12
 11
 10
 9
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 2
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DEBUG 25
 LCN4400

12
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 10
 9
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 5
 4
 3
 2
 1

DEBUG 26
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 27
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 28
 LCN4400

12
 11
 10
 9
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 5
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 3
 2
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DEBUG 29
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12
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 8
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 6
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DEBUG 30
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12
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 9
 8
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 3
 2
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DEBUG 31
 LCN4400

12
 11
 10
 9
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 5
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 3
 2
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DEBUG 32
 LCN4400

12
 11
 10
 9
 8
 7
 6
 5
 4
 3
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DEBUG 33
 LCN4400

12
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 8
 7
 6
 5
 4
 3
 2
 1

DEBUG 34
 LCN4400

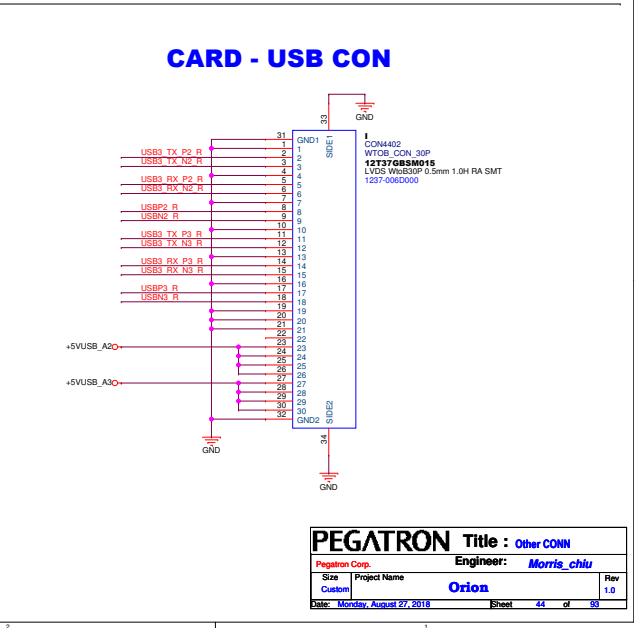
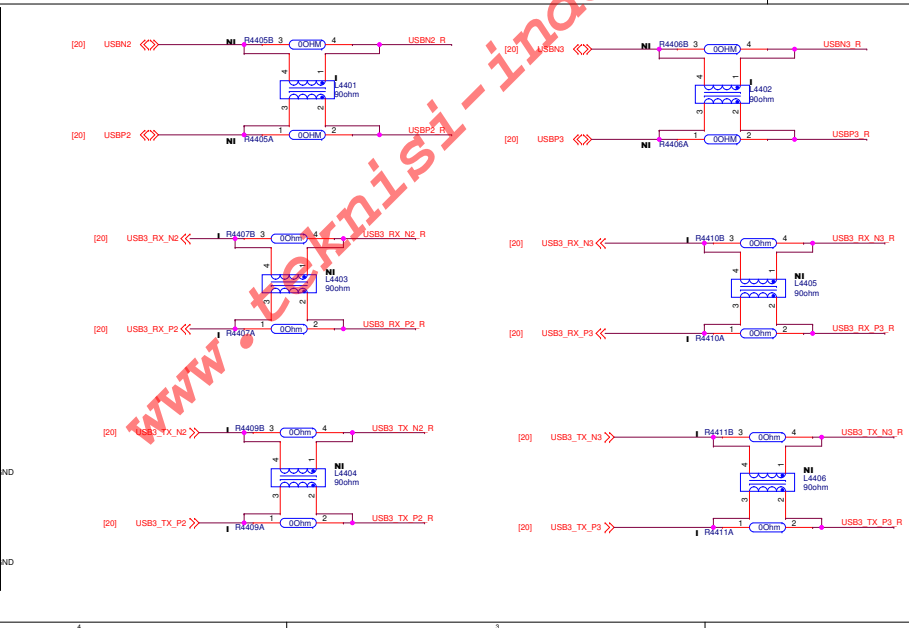
12
 11
 10
 9
 8
 7
 6
 5
 4

[illegible]

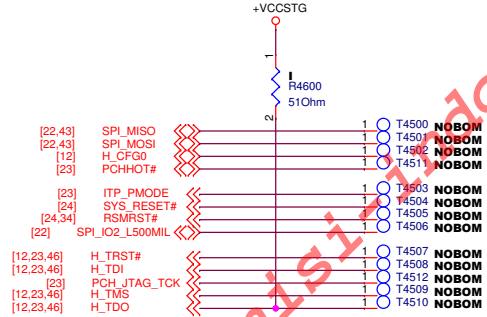
PWRBTN CONNECTOR

The diagram illustrates the internal circuitry of the PWRBTN connector. Key components and connections include:

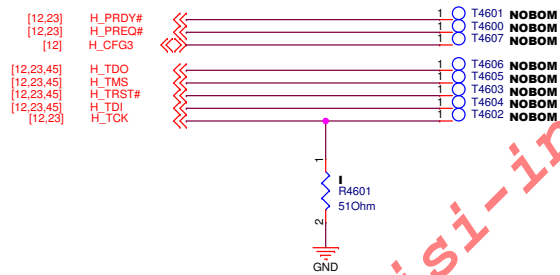
- Input Section:** A 3P2VA-EC connector is connected to a network of resistors (R4402, R4403, R4404) and capacitors (C4402, C4403). The output is labeled EC_PWRBTN.
- Output Section:** The PWRBTN pin is connected to a network of resistors (R4402, R4403, R4404) and capacitors (C4402, C4403). The output is labeled PWRBTN.
- Power Section:** A +5VA_PLED power source is connected to a network of resistors (R4402, R4403, R4404) and capacitors (C4402, C4403). The output is labeled PWR_LED.
- Grounding:** Multiple ground connections are shown, including GND and GND1.
- Component Values:** Resistors are labeled with values like 100K, 10K, and 100K. Capacitors are labeled with values like 100K, 10K, and 100K.
- Part Numbers:** Various part numbers are listed, including 12118000500, 12118001000, and 12118001000.
- Notes:** A note indicates that the connector is a 12-pin connector, with pins 1 through 12 labeled.

[illegible]

INTEL PCH DEBUG TESTPOINT



INTEL CPU DEBUG TESTPOINT



PEGATRON DT-MB RESTRICTED SECRET

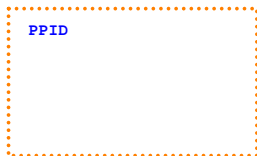
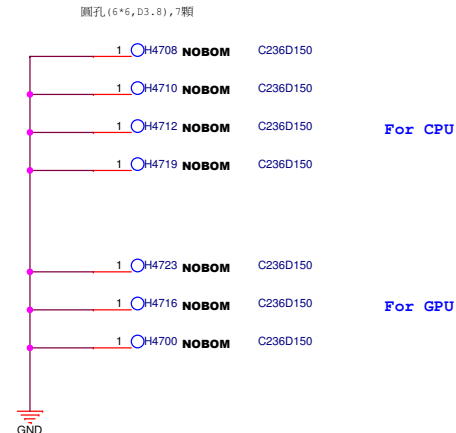
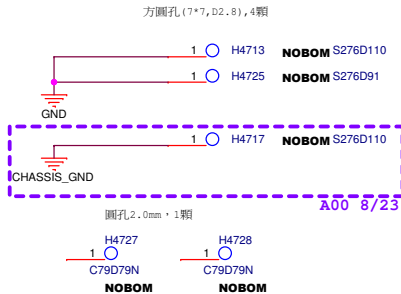
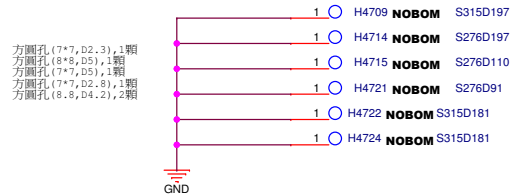
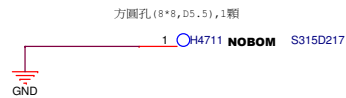
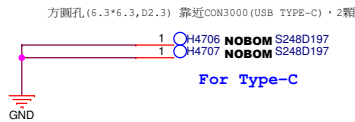
PEGATRON Title : DEBUG TESTPOINT(CPU)

Pegatron Corp. Engineer: **Morris_chiu**

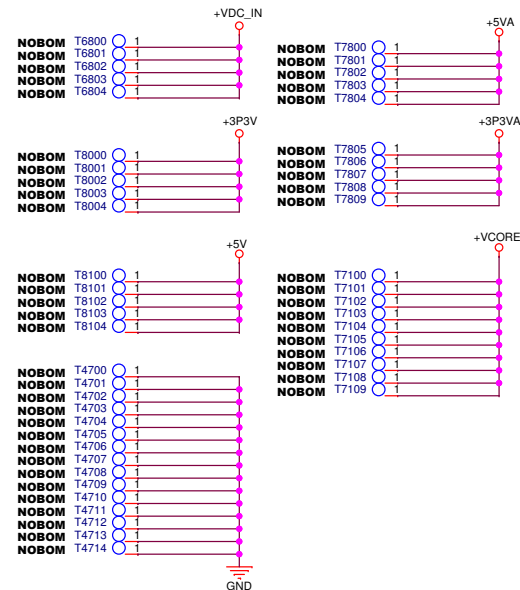
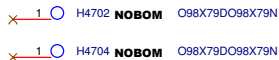
Size A3	Project Name Orion	Rev 1.0
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Date: **Monday, August 27, 2018** Sheet **46** of **93**

NI_TEMP
PCB4700
PCB
PCB_BOARD
CCL = Y

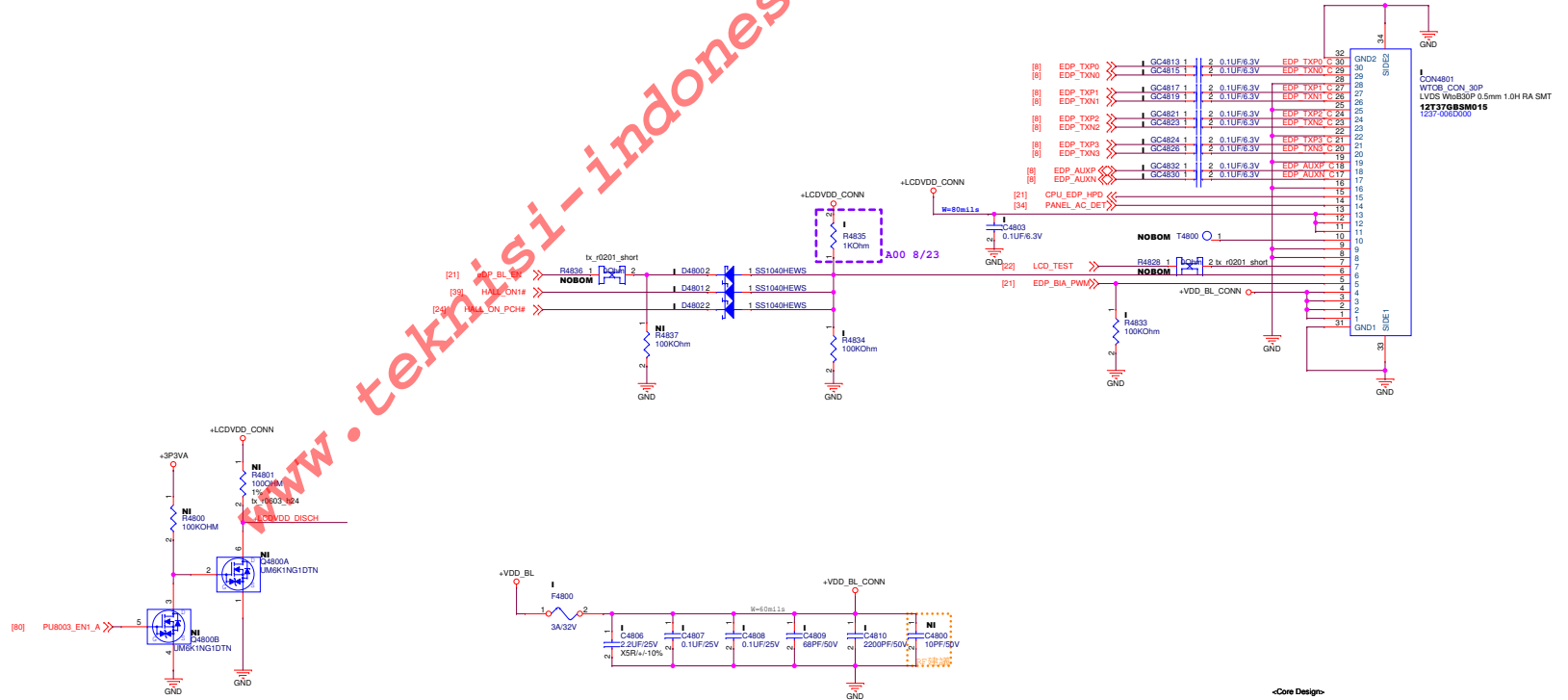


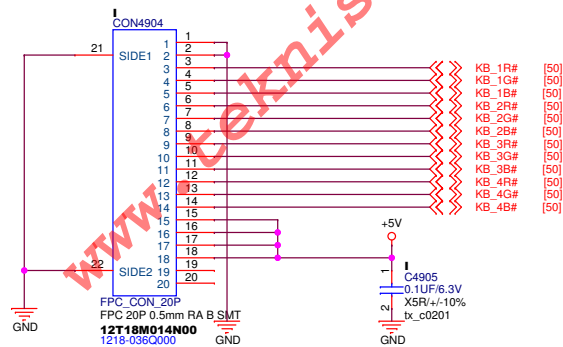
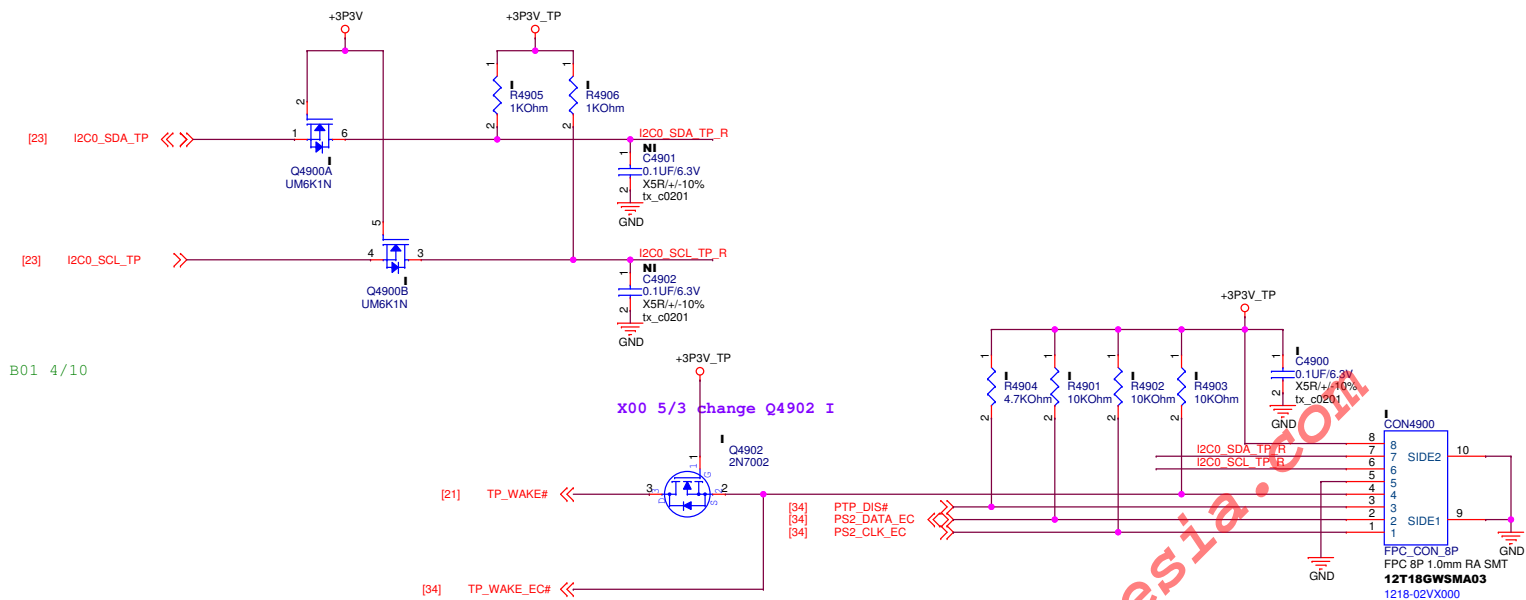
圓孔2.5mm*2.0mm * 2顆



PEGATRON DT-MB RESTRICTED SECRET

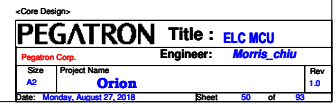
PEGATRON		Title : PCB & Label & Screw	
Pegatron Corp.		Engineer: Morris_chiu	
Size	Project Name	Date	Rev
A3	Orion	Monday, August 27, 2018	1.0
Date: Monday, August 27, 2018		Sheet	47 of 93





<Core Design>

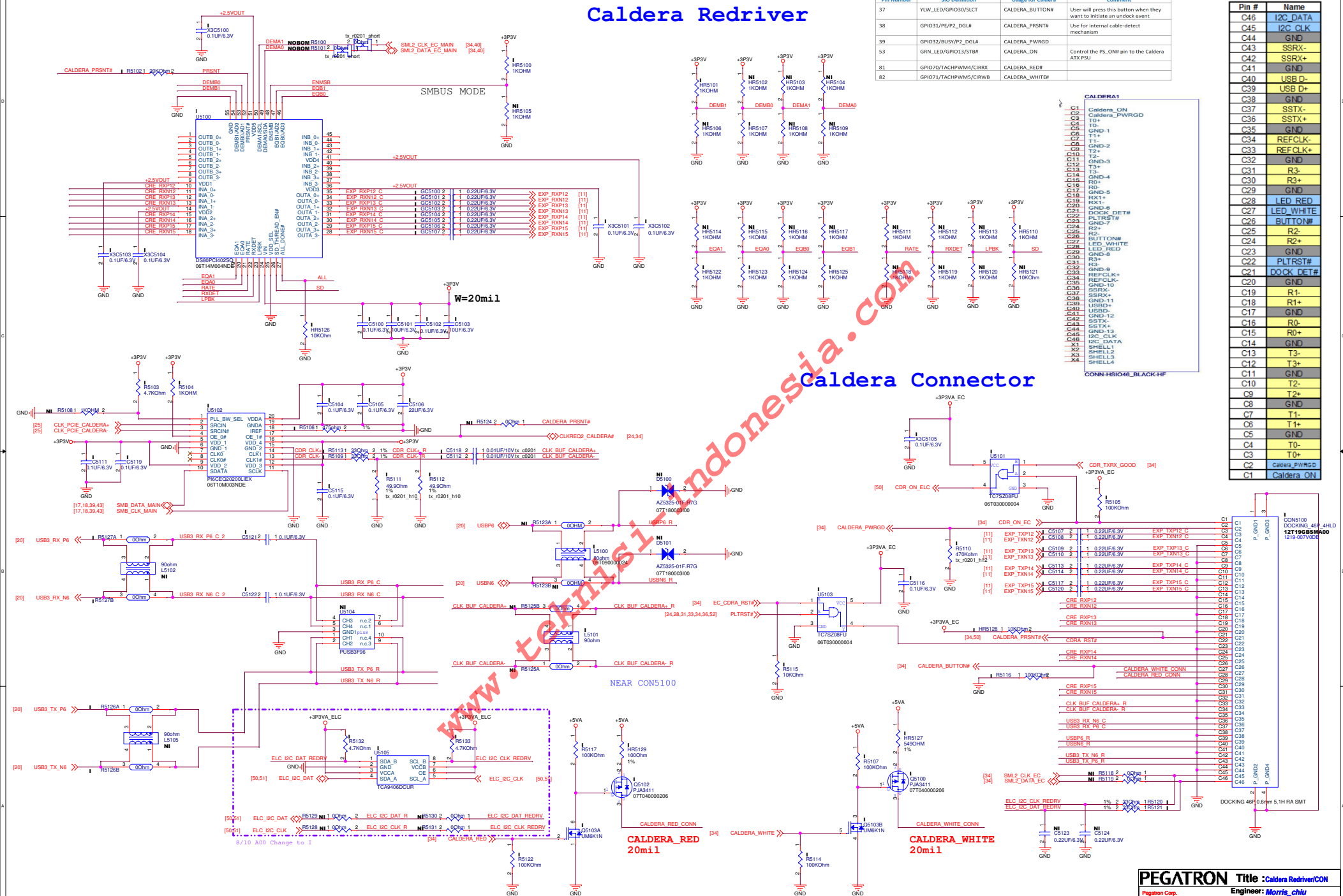
PEGATRON			Title : Touch & Keyboard BL
Pegatron Corp.			Engineer: Morris_chiu
Size A3	Project Name Orion		Rev 1.0
Date: Monday, August 27, 2018	Sheet	49	of 93

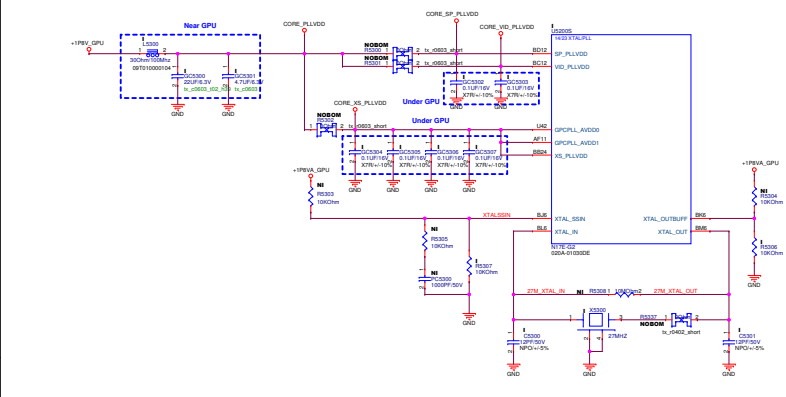


Caldera Redriver

Pin Number	SIO Definition	Usage for Caldera	Comment
37	YLV_LED/GPIO30/SLCT	CALDERA_BUTTON#	User will press this button when they want to initiate an undock event
38	GPIO31/PE/P2_DSL#	CALDERA_PSRST#	Use for internal cable-detect mechanism
39	GPIO32/BUSV/P2_DSL#	CALDERA_PWRGD	
53	GRN_LED/GPIO13/STBM	CALDERA_ON	Control the PS_ON# pin to the Caldera ATX PSU
81	GPIO73/TACHPMM5/CIRWB	CALDERA_RED#	
82	GPIO73/TACHPMM5/CIRWB	CALDERA_WHITE#	

Pin #	Name
C46	I2C_DATA
C45	I2C_CLK
C44	GND
C43	SSRX+
C42	SSRX+
C41	GND
C40	USB D-
C39	USB D+
C38	GND
C37	SSTX+
C36	SSTX+
C35	GND
C34	REFCLK-
C33	REFCLK+
C32	GND
C31	R+
C30	R+
C29	GND
C28	LED_RED
C27	LED_WHITE
C26	BUTTON#
C25	R+
C24	R+
C23	GND
C22	PLTRST#
C21	DOCK_DET#
C20	GND
C19	R+
C18	R+
C17	GND
C16	R+
C15	R+
C14	GND
C13	T+
C12	T+
C11	GND
C10	T+
C9	T+
C8	GND
C7	T+
C6	T+
C5	GND
C4	T+
C3	T+
C2	Caldera_PWRGD
C1	Caldera_ON

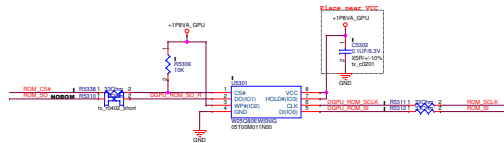
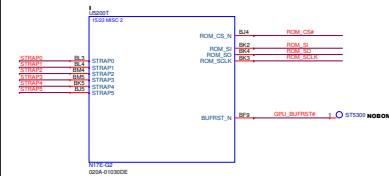




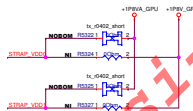
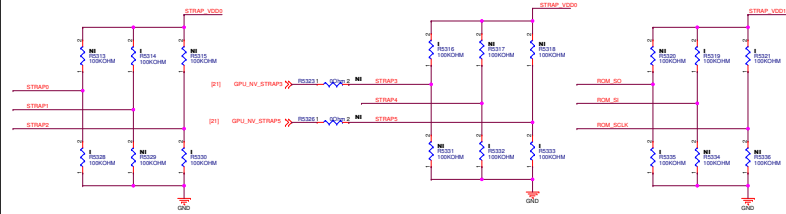
Total Display Links (HDMI, DP or DVI)				See This Row of Table 5.5	
		Is eDP Supported on:			
		IFPA or IFPB?	IFPC or IFPD?	IFPE or IFPF?	
4	4	--	--	--	15
4	3	yes	--	--	14
4	3	--	yes	--	13
4	3	--	--	yes	11
3	3	--	--	--	14
3	2	yes	--	--	12
3	2	--	yes	--	12
3	2	--	--	yes	10
2	2	--	--	--	12
2	1	yes	--	--	8
2	1	--	yes	--	8
2	1	--	--	yes	8
1	1	--	--	--	8
1	0	yes	--	--	0
1	0	--	yes	--	0
1	0	--	--	yes	0

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
All other Strap Configurations				(Reserved; do not configure)			
				(Reserved)			

Straps 需確認strap及ROM(Memory 還未確定)



Need NV check



STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
ROM_SO			1-ENABLE 0-DISABLE
ROM_SI			1111 DEFAULT SOR01/2/3 ENABLE
L	L	L	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000
STRAPS			SMB_ALT_ADDR
M	H	H	1
M	H	L	1
M	L	H	1
M	L	L	1
L	H	M	1
L	M	H	1
L	M	L	1
L	L	M	1
L	L	L	1
H	H	H	0
H	H	L	0
H	L	H	0
H	L	L	0
L	H	H	0
L	H	L	0
L	L	H	0
L	L	L	0
			DEVID_SEL
M	H	H	1
M	H	L	1
M	L	H	1
M	L	L	1
L	H	M	1
L	M	H	1
L	M	L	1
L	L	M	1
L	L	L	1
H	H	H	0
H	H	L	0
H	L	H	0
H	L	L	0
L	H	H	0
L	H	L	0
L	L	H	0
L	L	L	0
			PCIE_CFG
M	H	H	1
M	H	L	1
M	L	H	1
M	L	L	1
L	H	M	1
L	M	H	1
L	M	L	1
L	L	M	1
L	L	L	1
H	H	H	0
H	H	L	0
H	L	H	0
H	L	L	0
L	H	H	0
L	H	L	0
L	L	H	0
L	L	L	0
			VGA_DEVICE
M	H	H	1
M	H	L	1
M	L	H	1
M	L	L	1
L	H	M	1
L	M	H	1
L	M	L	1
L	L	M	1
L	L	L	1
H	H	H	0
H	H	L	0
H	L	H	0
H	L	L	0
L	H	H	0
L	H	L	0
L	L	H	0
L	L	L	0

H-High :Tied to 1.8V
M-Middle:Tied to 0.9V
L-Low :Tied to 0V

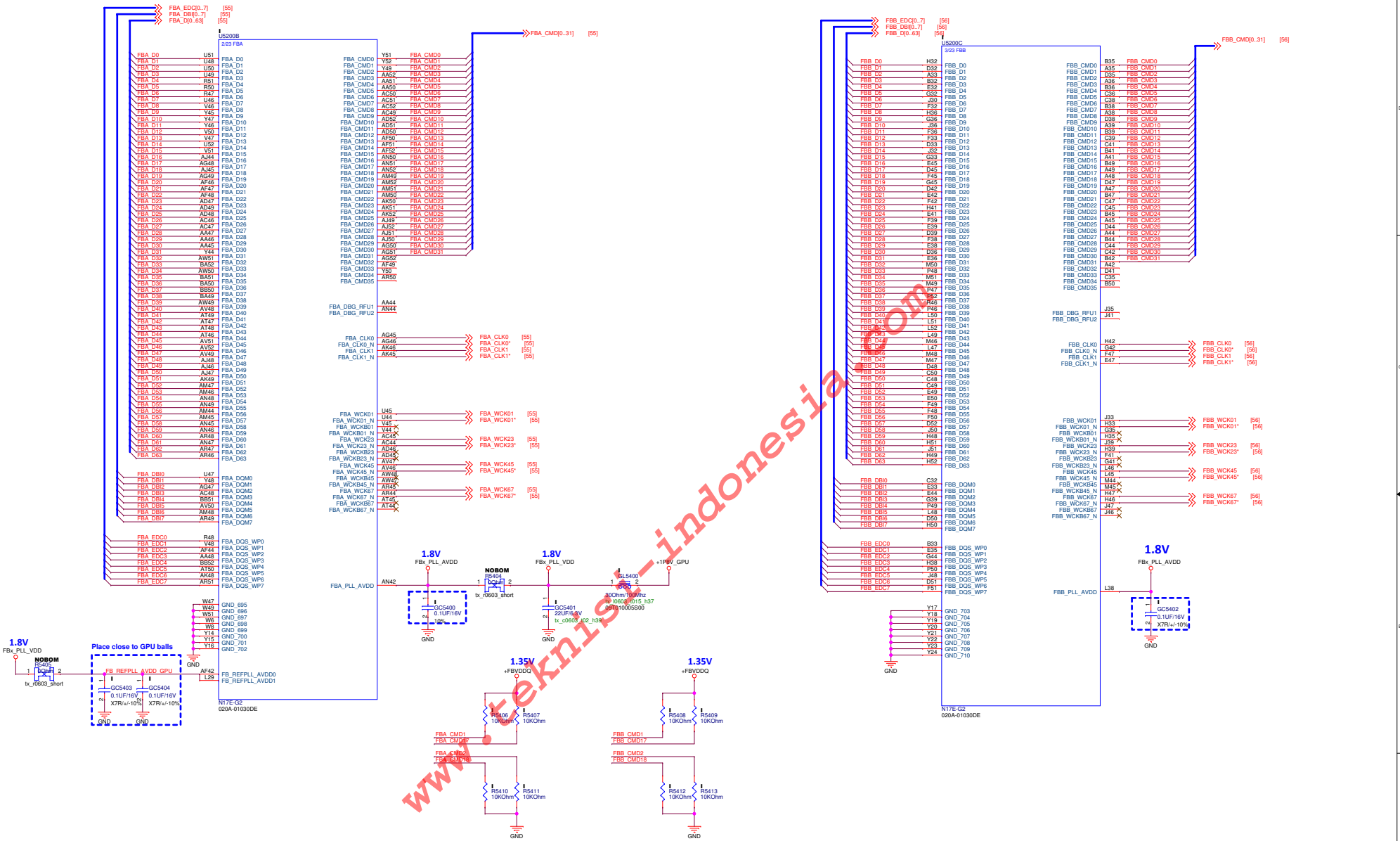
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	
L	L	H	1 (0x0001)	
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

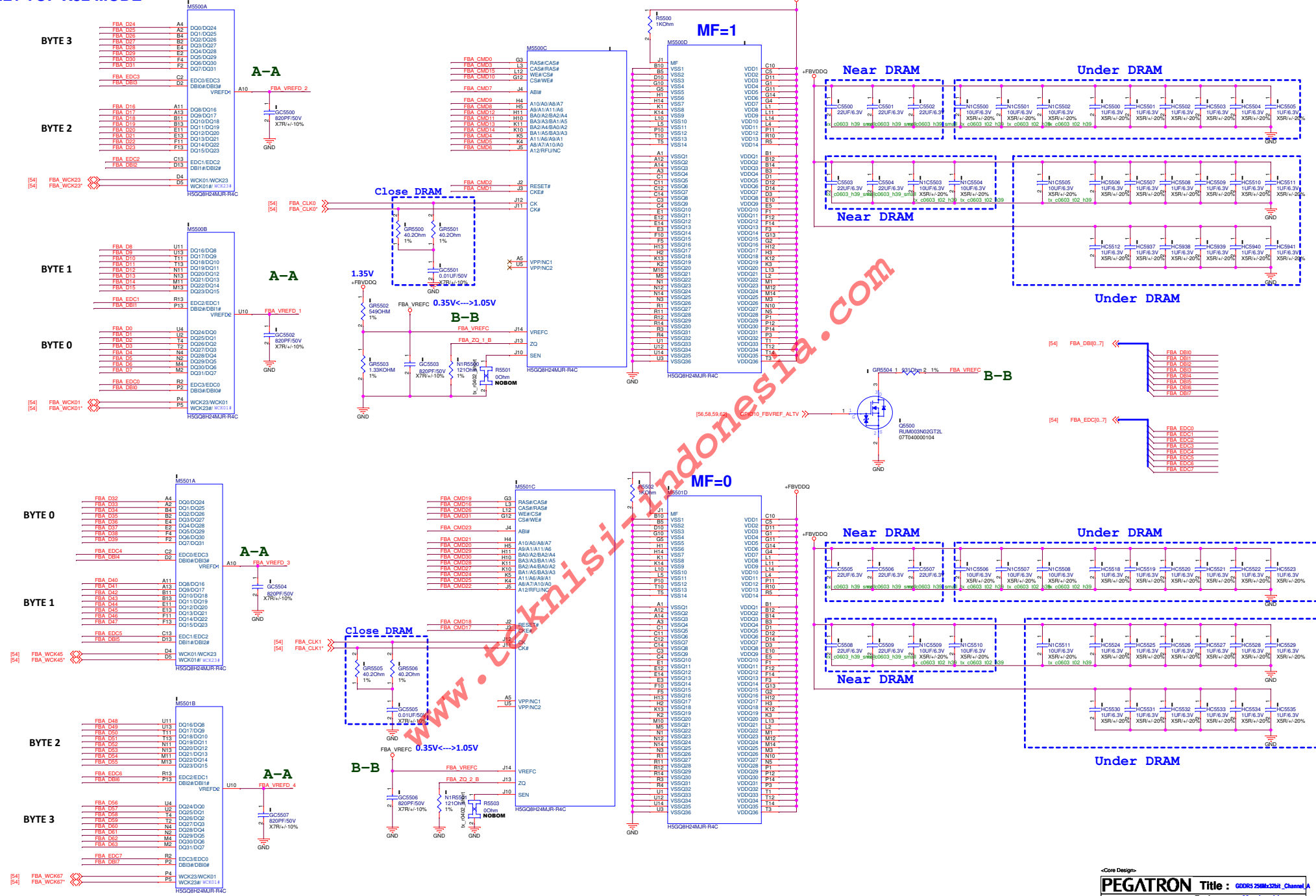
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alias	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.55V	Samsung	K4G03225F-HC25	B-die	0x0	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V	Hynix	H5GQ8440R-R0C	0x0	0x1	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V			0x0	0x2	8 Gbps	N/A	Full	Post production candidate

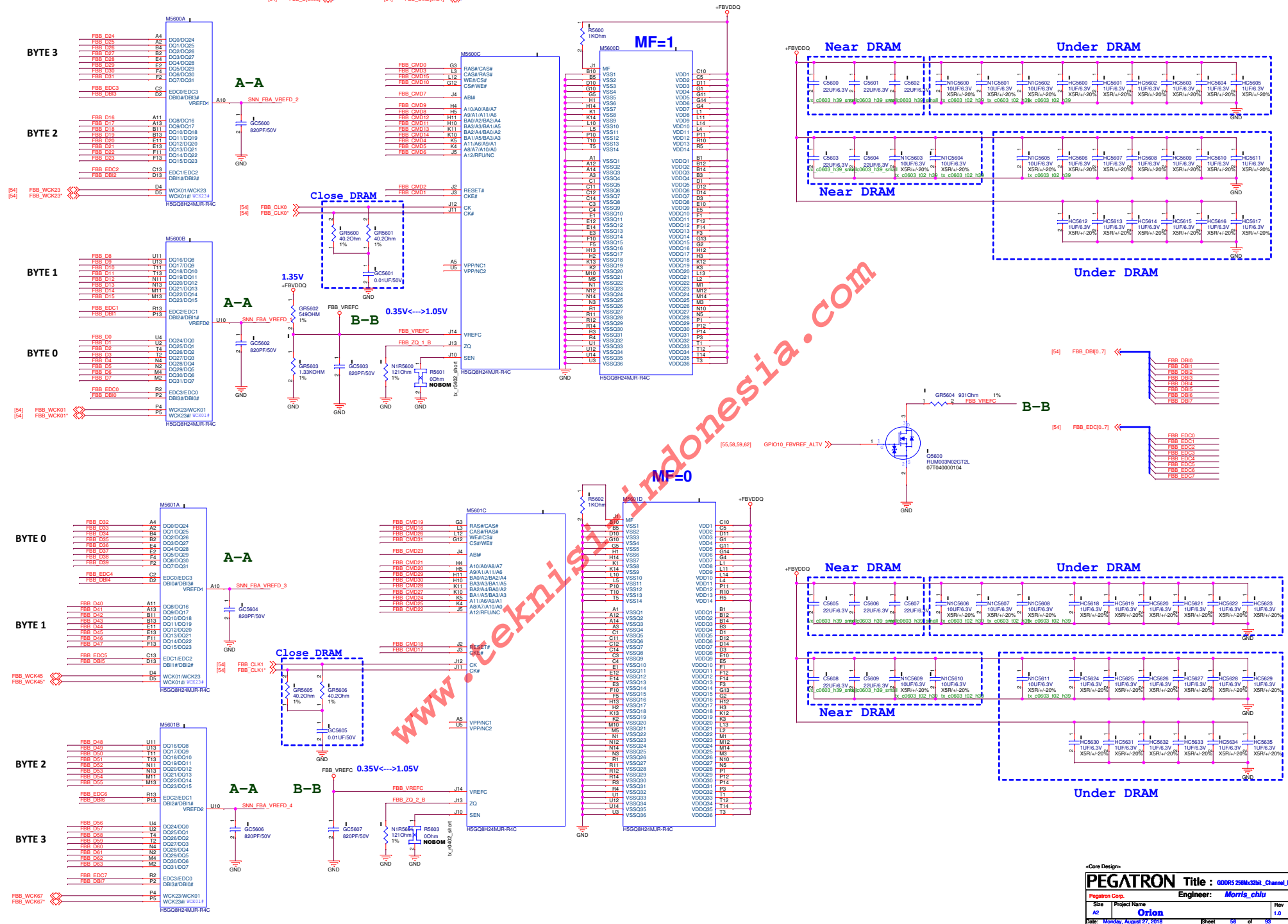
PEGATRON DT-MB RESTRICTED SECRET

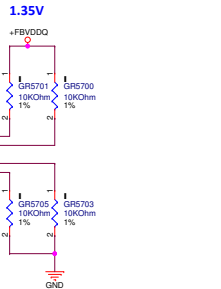
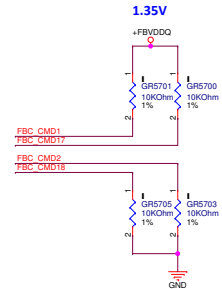
PEGATRON		Title : GPU-Rel & Straps	
Engineer: Morris_chen		Date: 2016-05-17	
Rev: 1.0	Project Name: Oryon	Date: 2016-05-17	

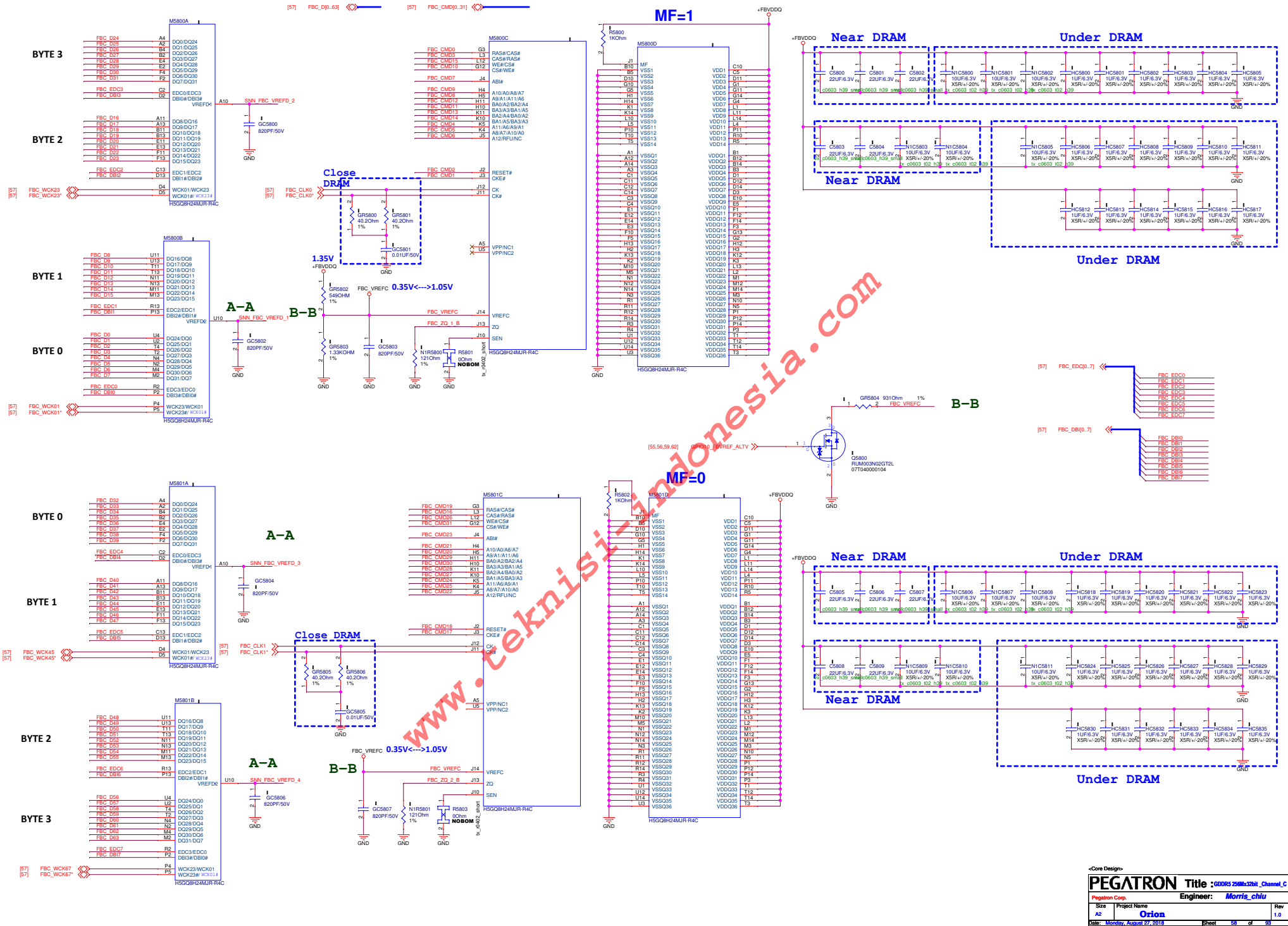


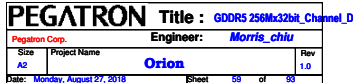
CELL1 TOP X32 MODE



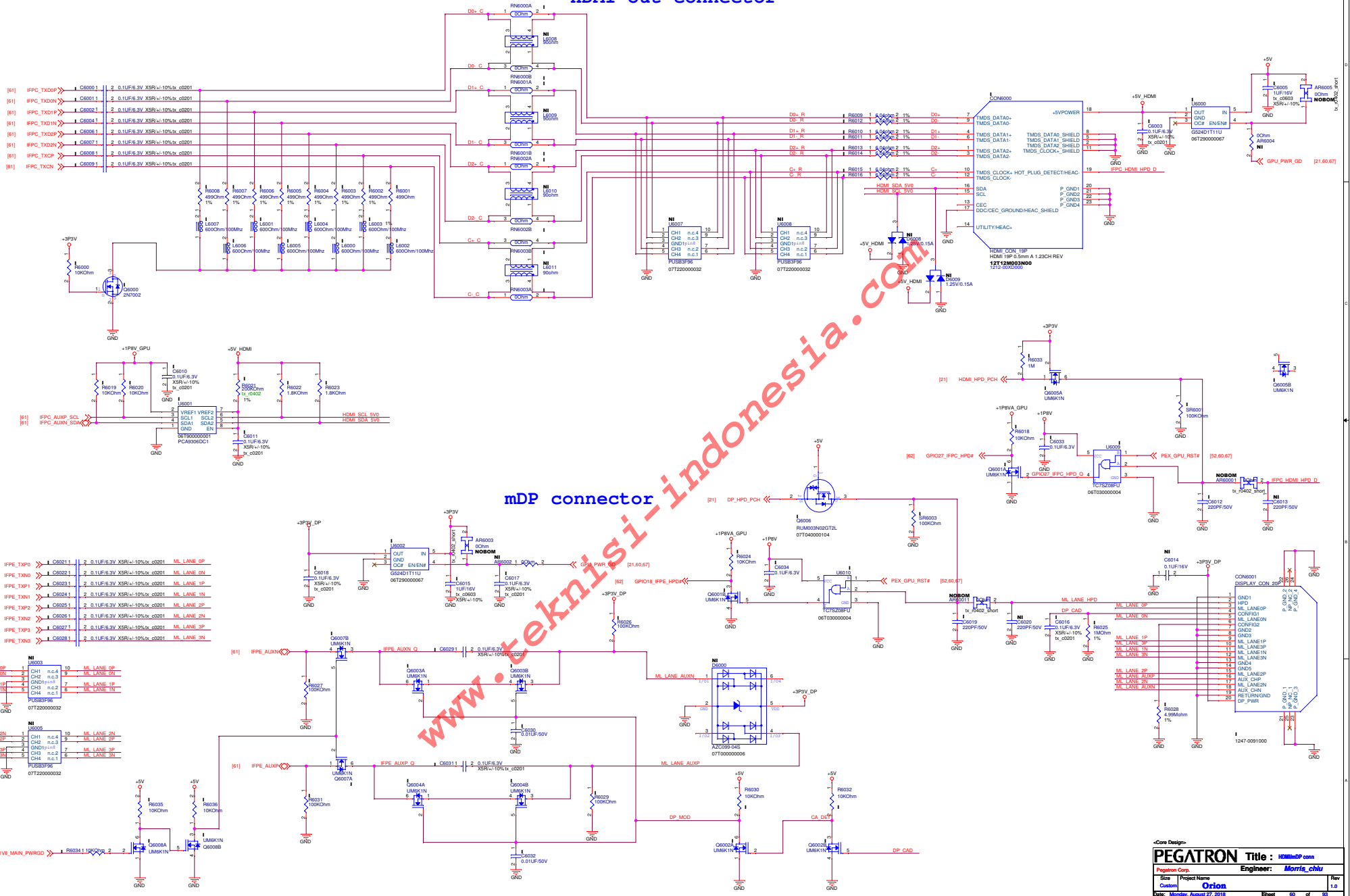


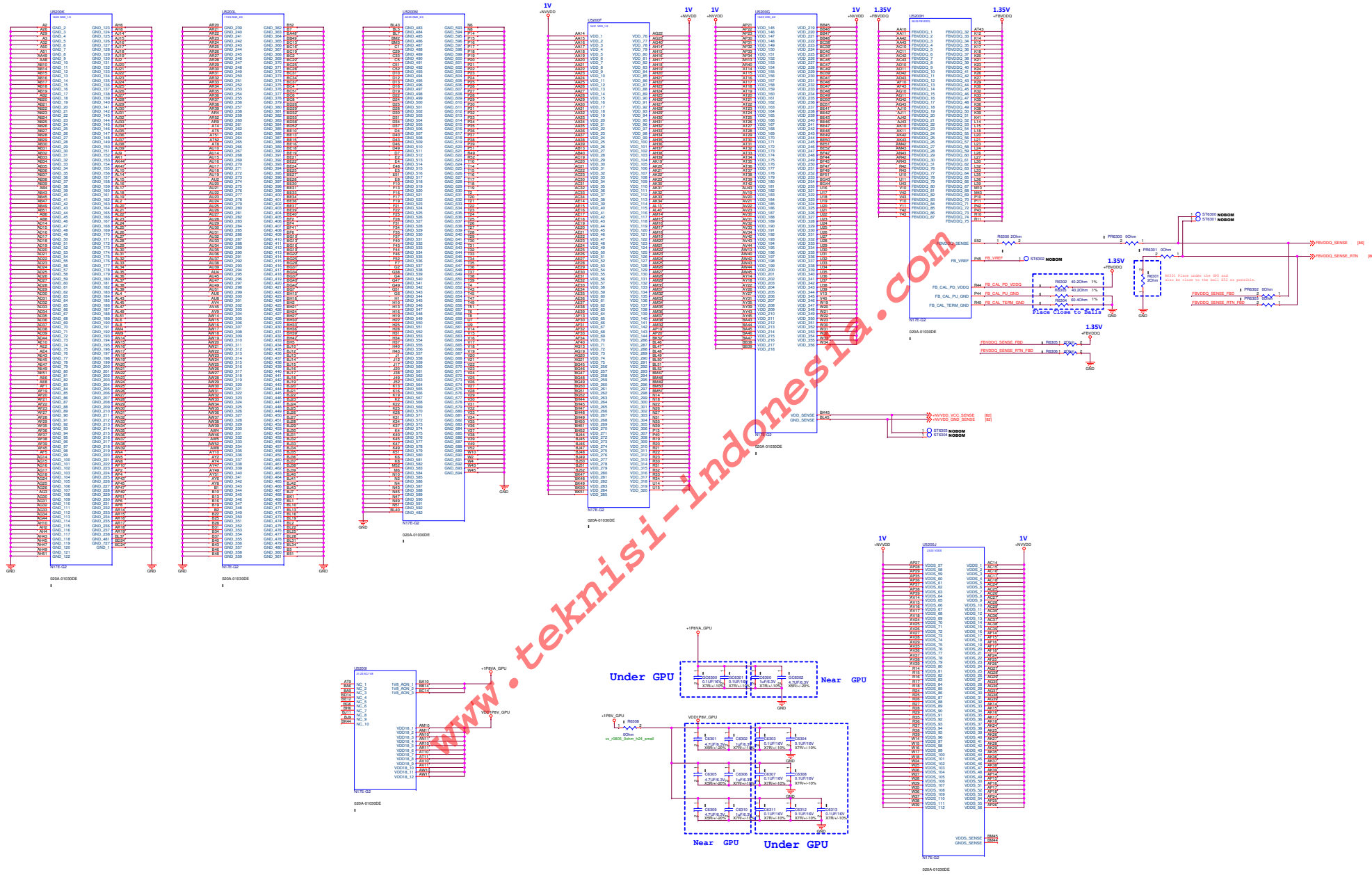




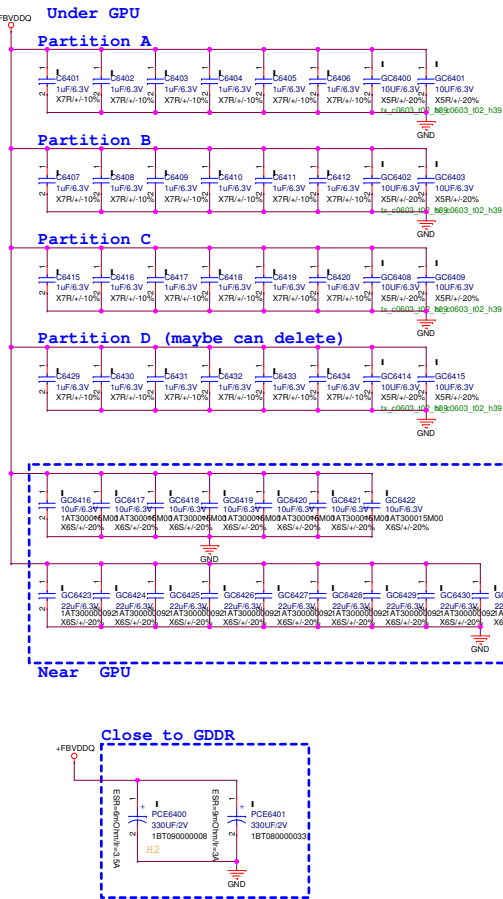


HDMI out connector





+FBVDDQ



+NVVDD



+NVVDD

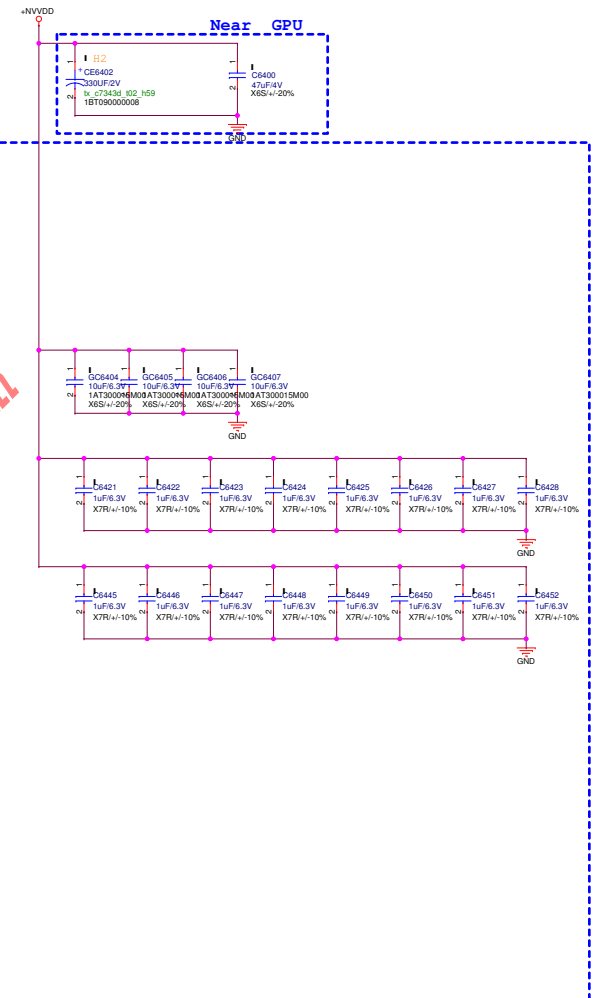
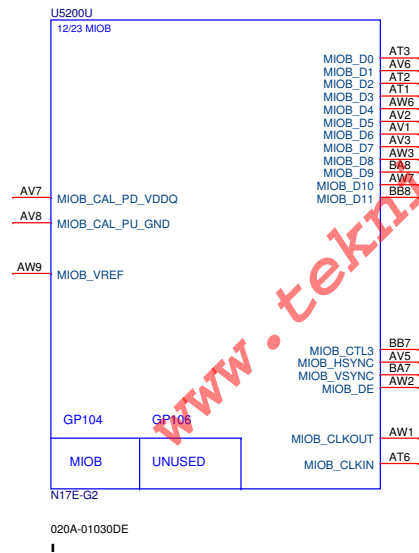
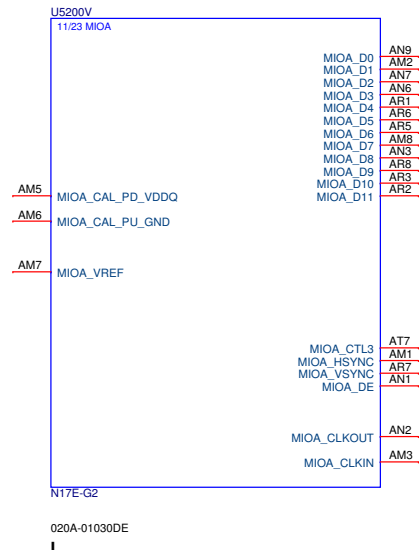
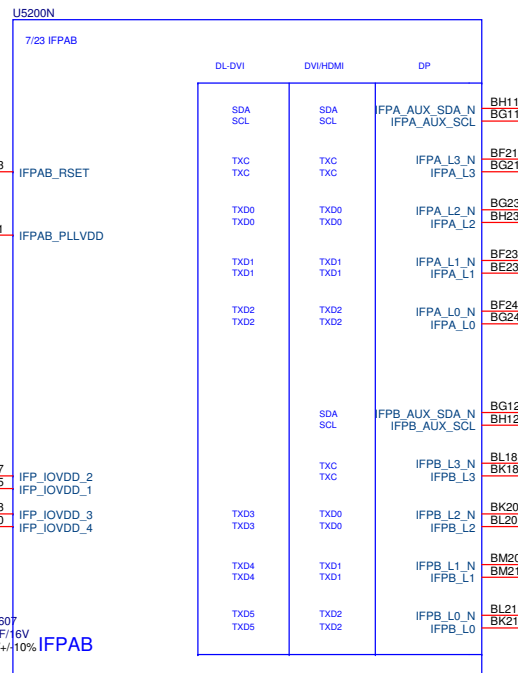
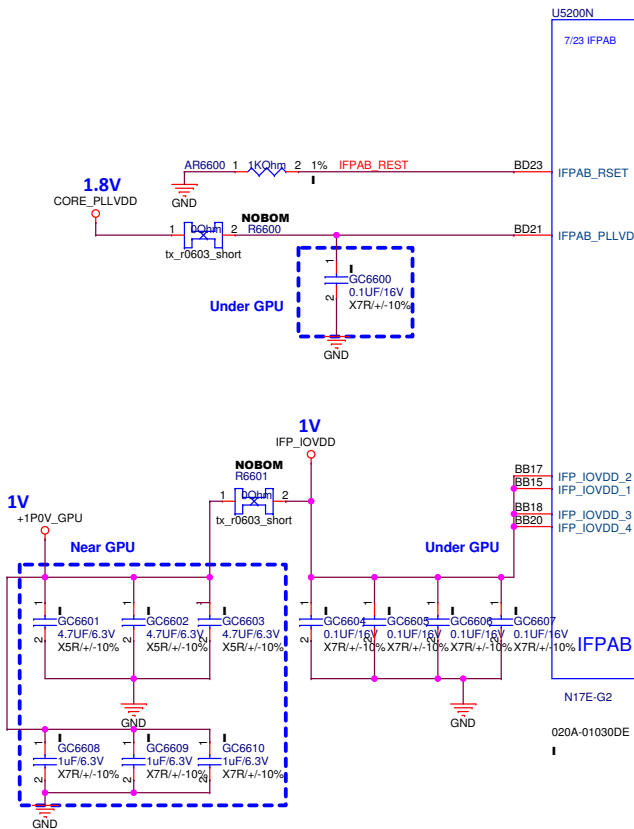


Table 11. NVVDD and NVVDDS Power Rail Filtering

Rail (GPU Ball) Name	Voltage	Filtering under GPU	Filtering near GPU
NVVDD +NVVDDS (Merge)	Varies	65 × 1 uF (0402 X6S) 15 × 10 uF (0603 X6S) 4 × 22 uF (0805 X6S) 2 × 47 uF (0805 X6S)	3 × 330 uF (Poscap) 1 × 47 uF (0805 X6S)
NVVDD (Split)	Varies	49 × 1 uF (0402 X6S) 11 × 10 uF (0603 X6S) 4 × 22 uF (0805 X6S) 2 × 47 uF (0805 X6S)	2 × 330 uF (Poscap)
NVVDDS (Split)	Varies	16 × 1 uF (0402 X6S) 4 × 10 uF (0603 X6S)	1 × 330 uF (Poscap) 1 × 47 uF (0805 X6S)

Core Design

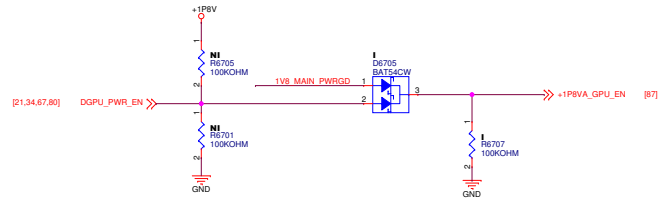




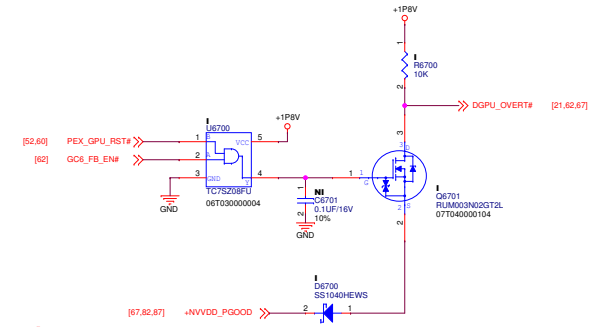
N17E-G2
020A-01030DE

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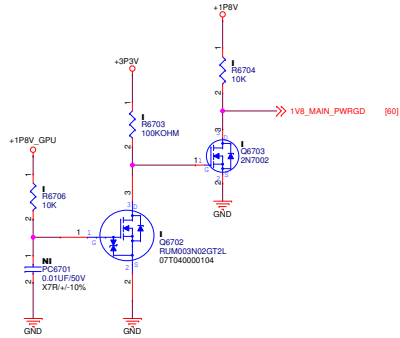
+1P8VA_GPU



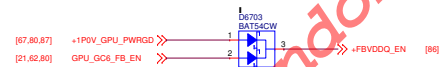
NVDD POWER GOOD LOOPBACK



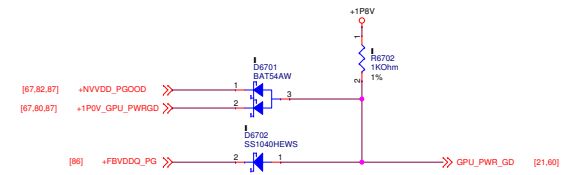
1V8_MAIN POWER GD



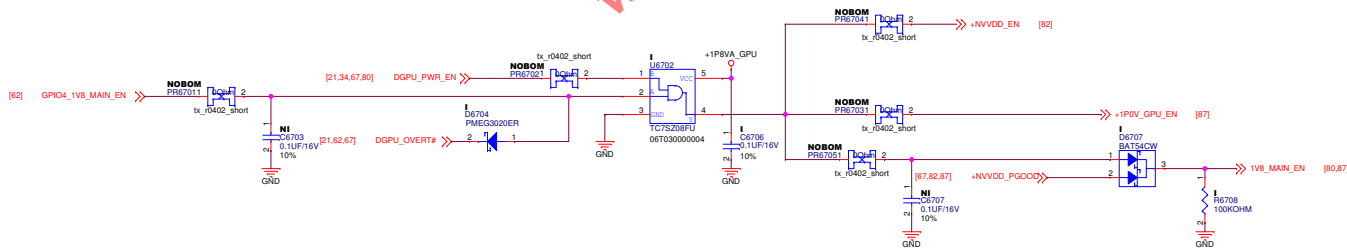
FBVDDQ Enable



BOARD GOOD

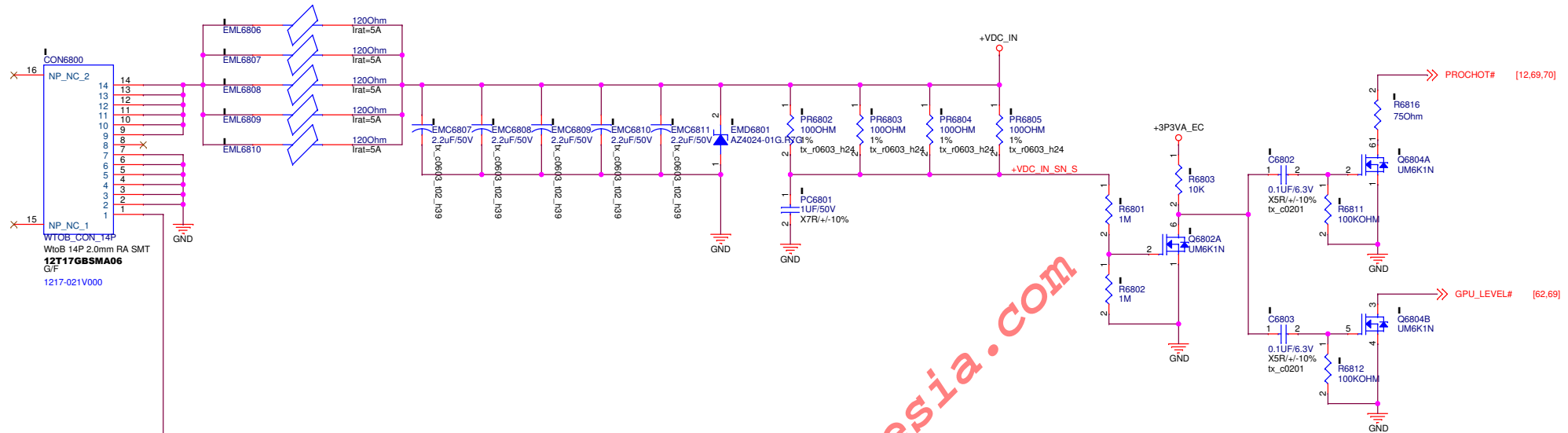


NVDD & PEX_VDD Enable

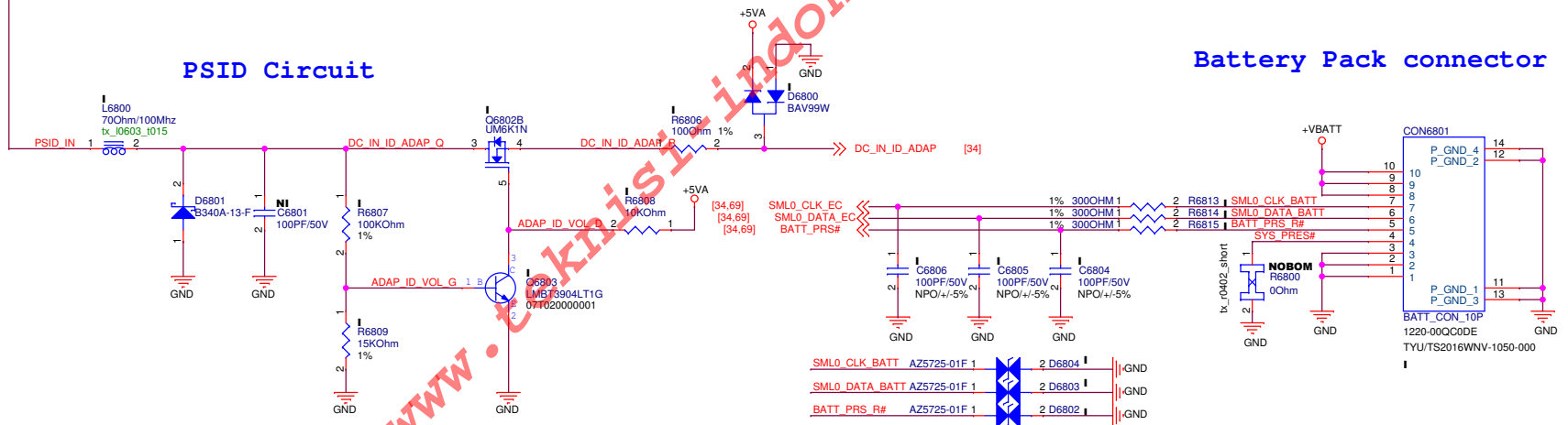


DC-IN connector

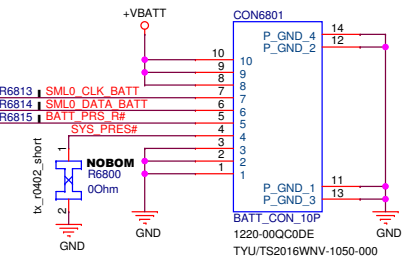
lin.cont= 12.31A
lin.peak=13.33A@4s



PSID Circuit

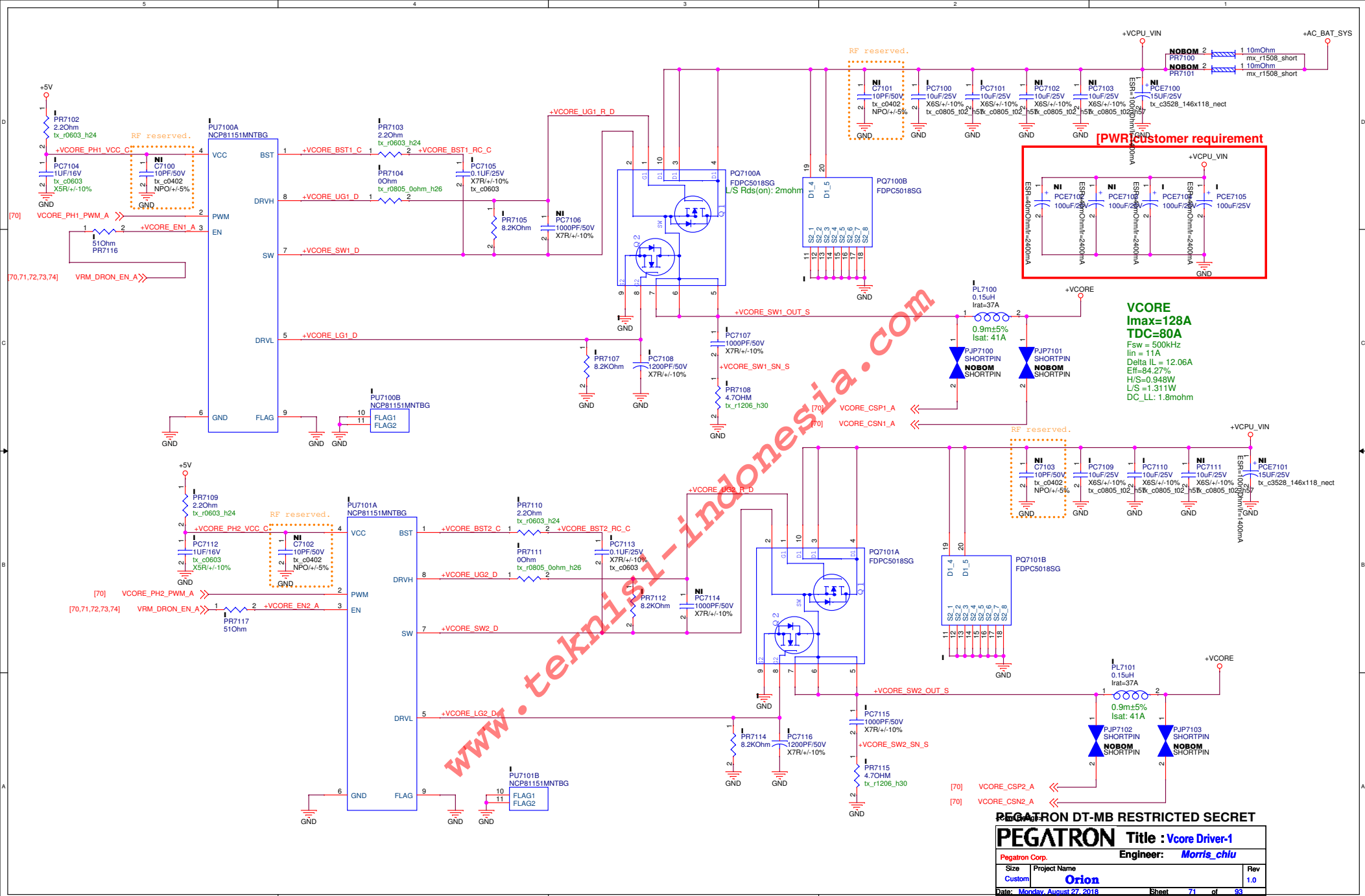


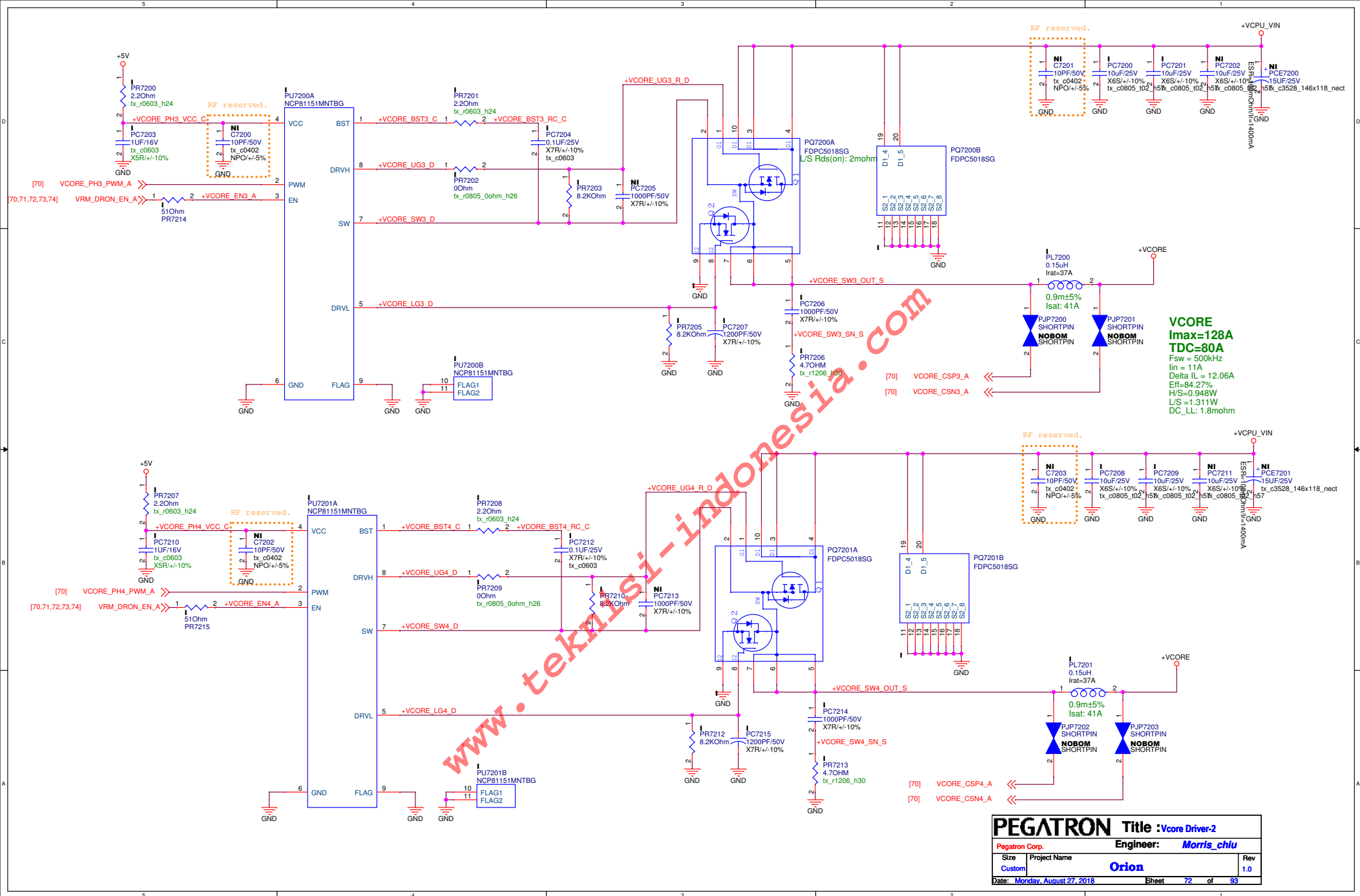
Battery Pack connector

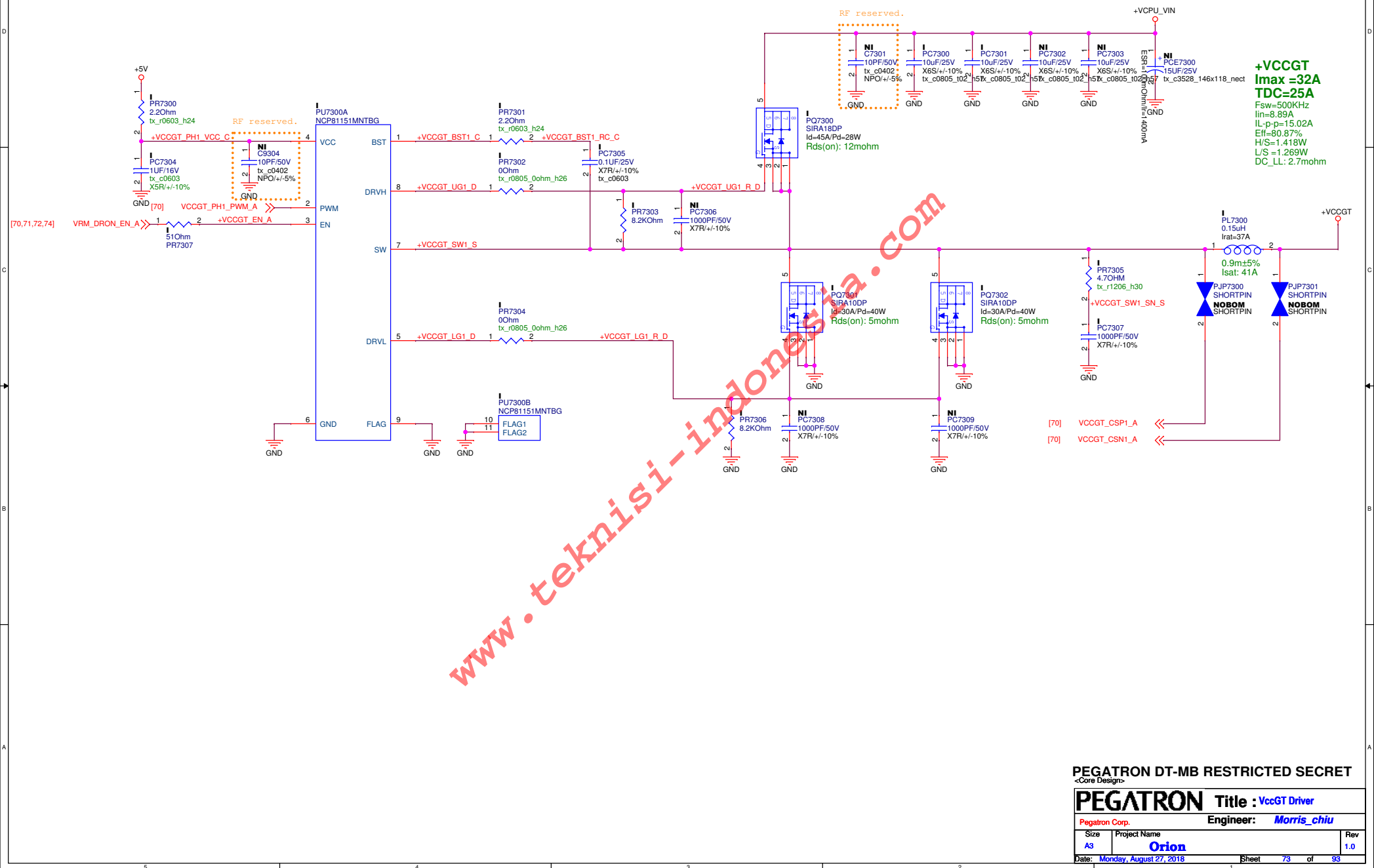


<Core Design>

PEGATRON Title : DC_IN		
Pegatron Corp.		Engineer: Morris_chiu
Size	Project Name	Rev
A3	Orion	1.0
Date: Monday, August 27, 2018	Sheet 68	of 93





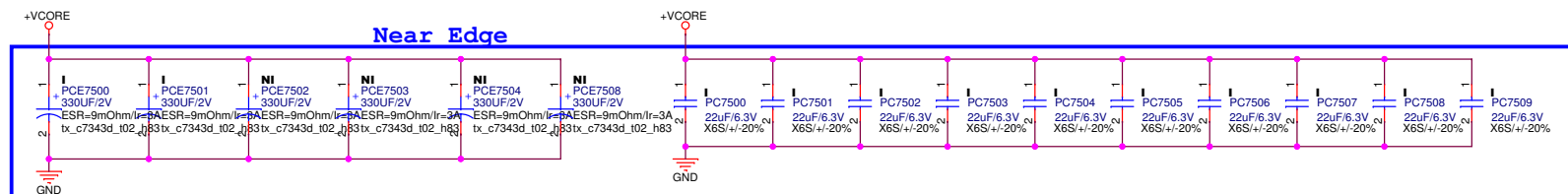


PEGATRON DT-MB RESTRICTED SECRET
<Core Design>

PEGATRON Title : VccGT Driver

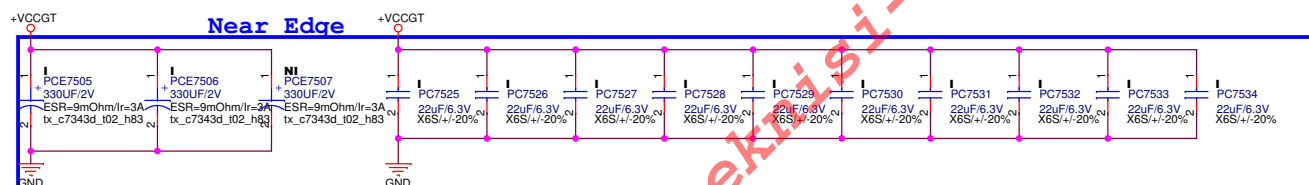
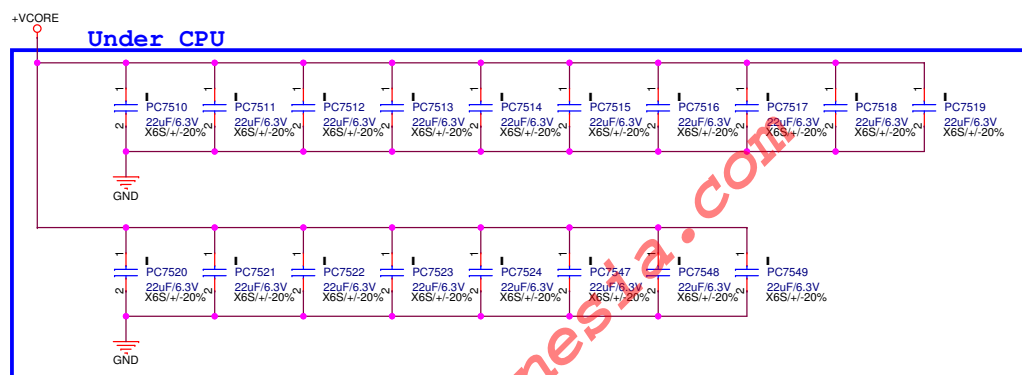
Pegatron Corp. Engineer: **Morris_chiu**

Size A3	Project Name Orion	Rev 1.0
Date: Monday, August 27, 2018		Sheet 73 of 93



Vcore Output CAP

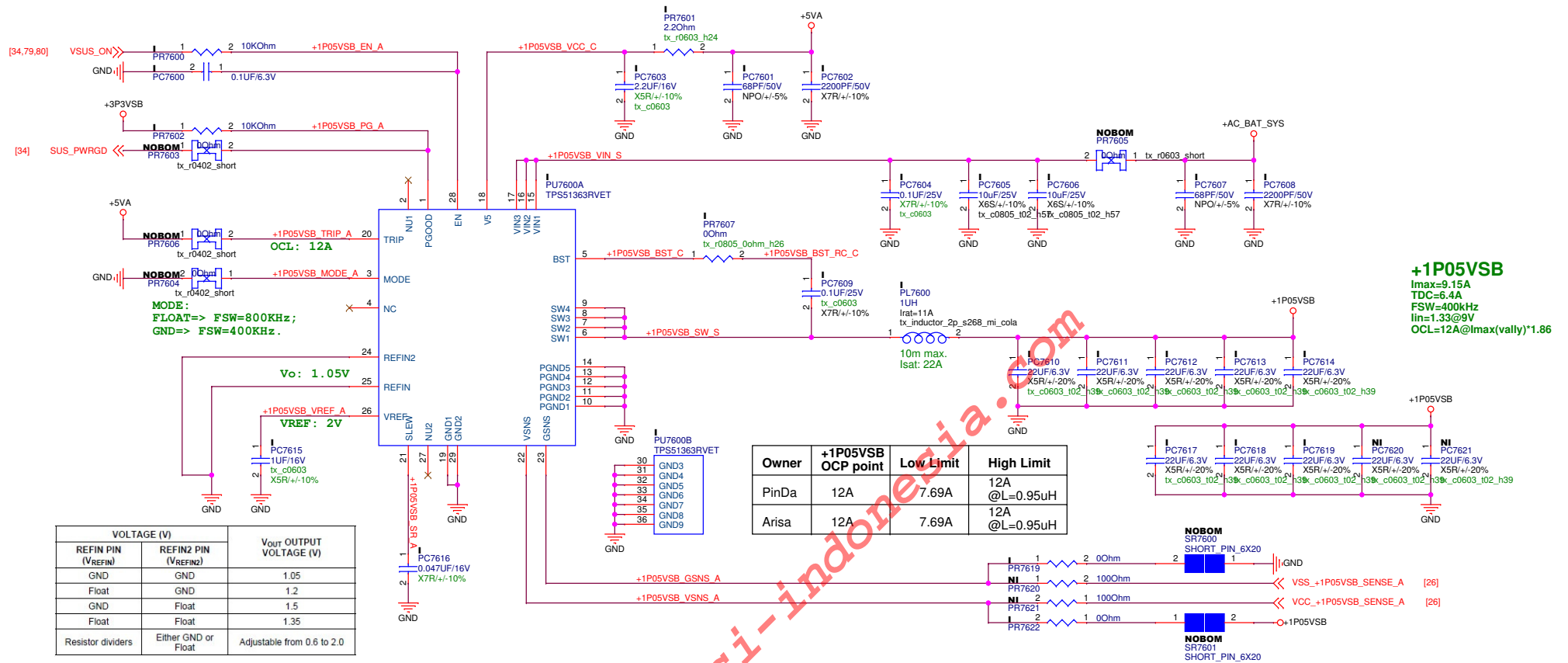
330uF/2V * 4 pcs
22uF/6.3V * 28pcs



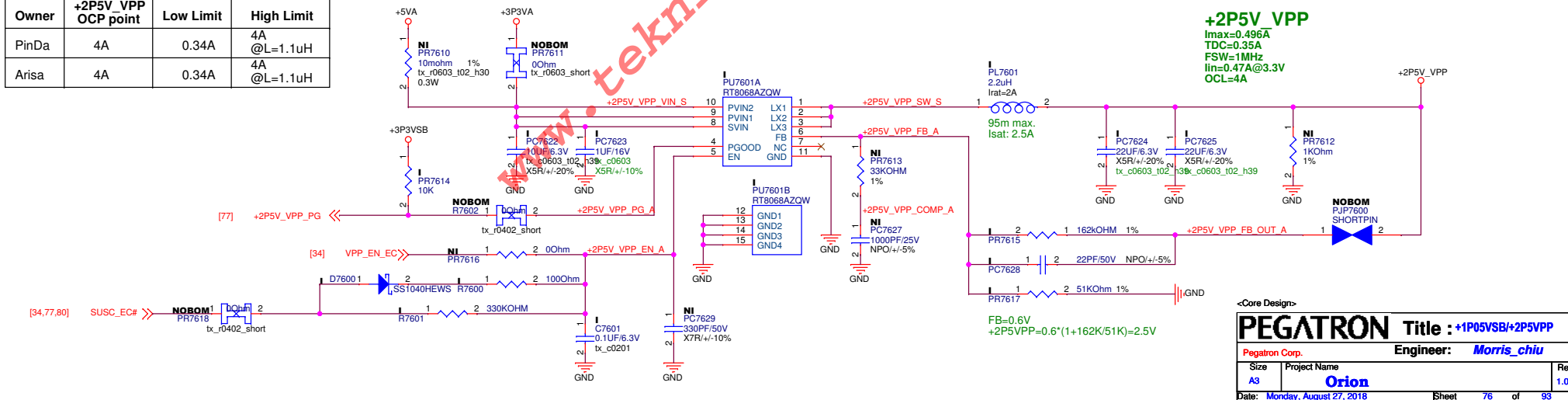
VCCGT Output CAP

330uF/2V * 3
22uF/6.3V * 22 pcs

PEGATRON		Title : Vcore & VccGT CAP	
Pegatron Corp.		Engineer: Morris_chiu	
Size A3	Project Name Orion	Date: Monday, August 27, 2018	Rev 1.0
		Sheet 75 of 93	



Owner	+2P5V_VPP OCP point	Low Limit	High Limit
PinDa	4A	0.34A	4A @L=1.1uH
Arisa	4A	0.34A	4A @L=1.1uH



+VTT_DDR
 Imax=1.5A
 TDC:1.05A

VTT LDO: 2A
 OCP:
 $QCP = 75 \times 10 / (8 / (3 \times 1.3) + (7.99 / 2)) = 28.03A @ 105 \text{ deg}$
 $QCP = 75 \times 10 / (8 / 3 + (7.99 / 2)) = 35.24A @ 25 \text{ deg}$

+3PVSBO
 VDDQ_PWROD

Owner	+1P2V_DUAL OCP point	Low Limit	High Limit
PinDa	35.24A@25 deg 28.03A@105 deg	16A	35.24A @L=0.32uH
Arisa	35.24A@25 deg 28.03A@105 deg	16A	35.24A @L=0.32uH

[34.39.62] SML1_DATA_EC
 [34.39.62] SML1_CLK_EC

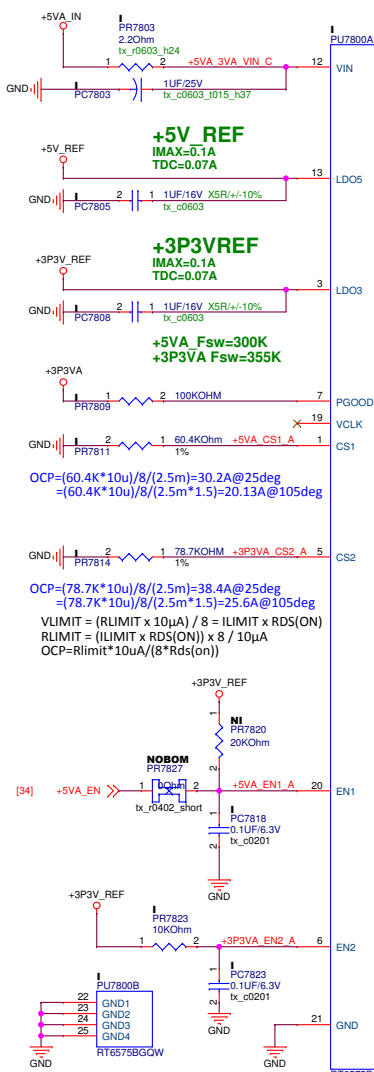
DAC

ExtReference Vref2

$$V_{out} = 1.8 \times (R2 / (R1 + R2)) = 1.8 \times (21K / (21K + 21K)) = 1.22V$$

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+1P2V_DUAL
 Imax=15.86A
 TDC=11.13A
 Iin=2.5@9V
 FSW=300kHz
 delta_IL=7.99A
 Vripple=35.94mV
 H/S=0.427W
 L/S=0.653W



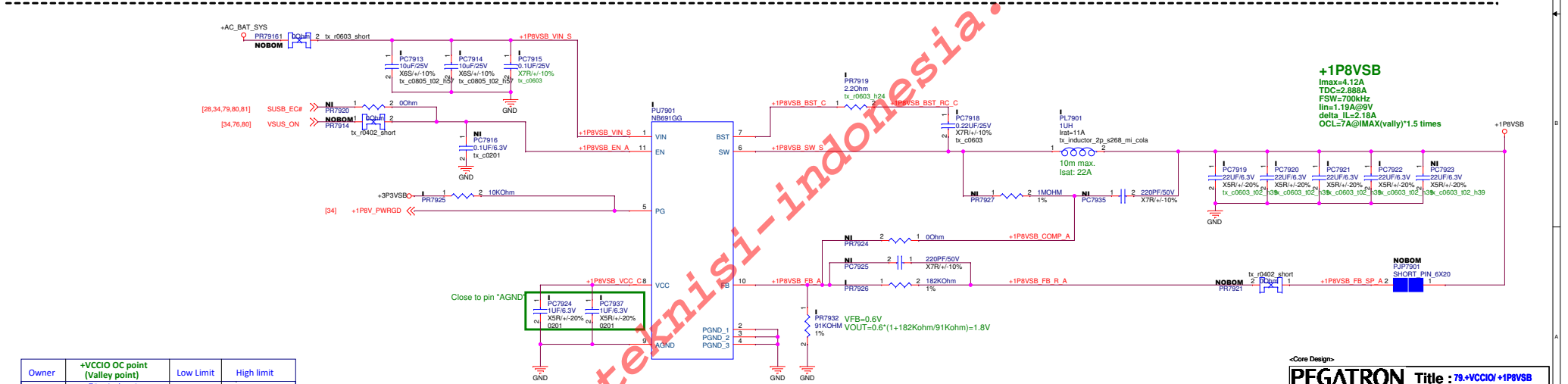
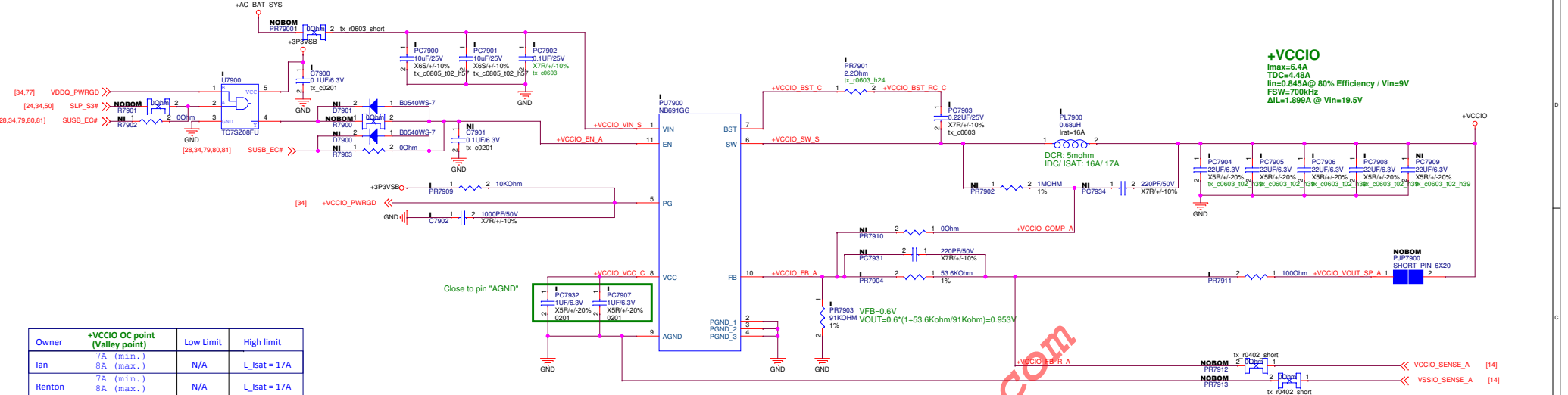
X01 7/18

PEGATRON Title :+3VA /+5VA

Pegatron Corp. Engineer: Morris.chiu

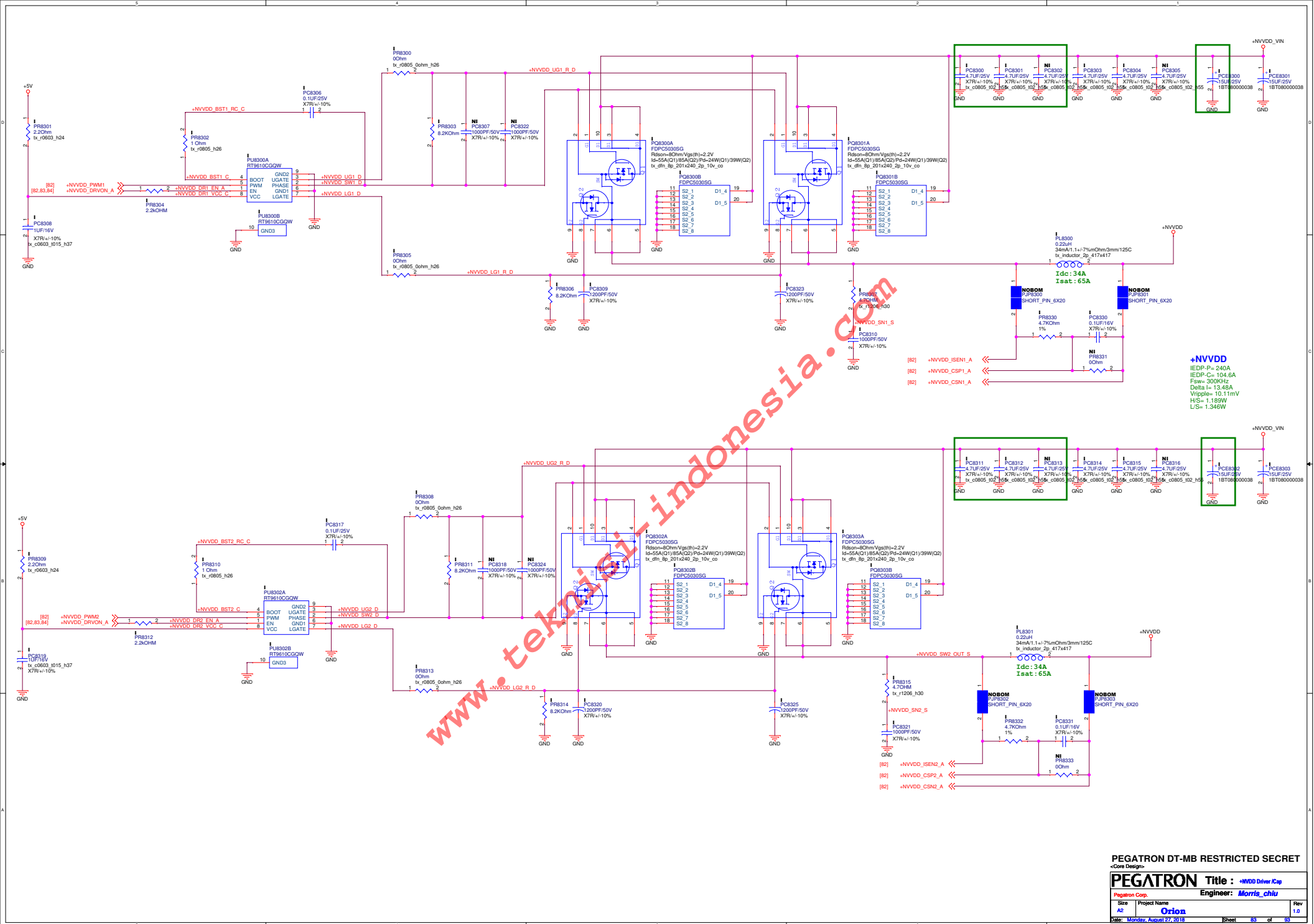
Size Project Name Orion Rev 1.0

Date: Monday, August 27, 2018 Sheet 78 of 93



<Core Design>

PEGATRON		Title : 79.+VCCIO/+1P8VSB	
Pegatron Corp.		Engineer: Morris_chiu	
Size	Project Name		Rev
Custom	Orion		1.0
Date: Monday, August 27, 2018		Sheet	79 of 83



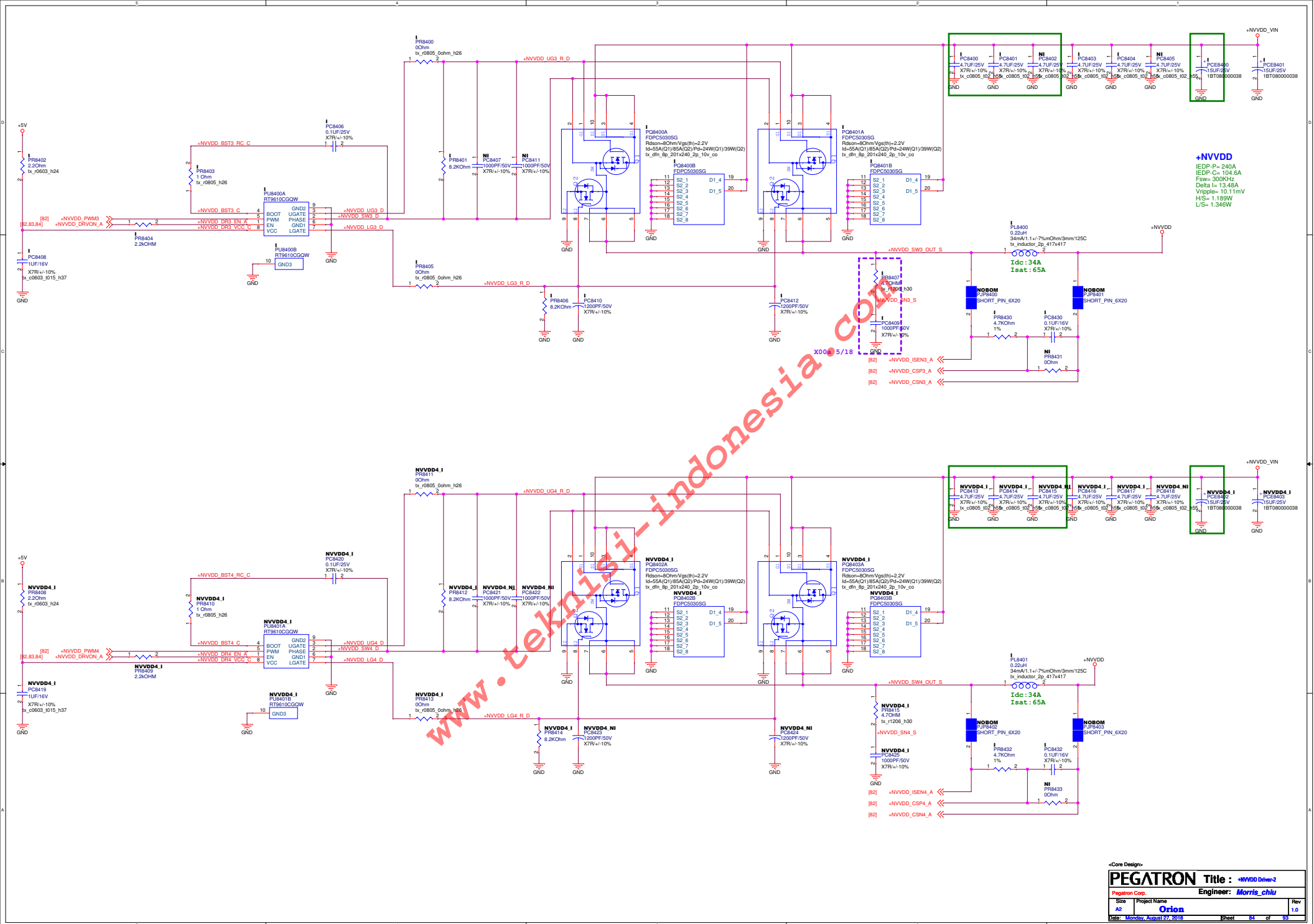
PEGATRON DT-MB RESTRICTED SECRET
Core Design

PEGATRON Title : +NVDD Driver Cap

Engineer: Morris_chu

Size	Project Name	Rev
A2	Orion	1.0

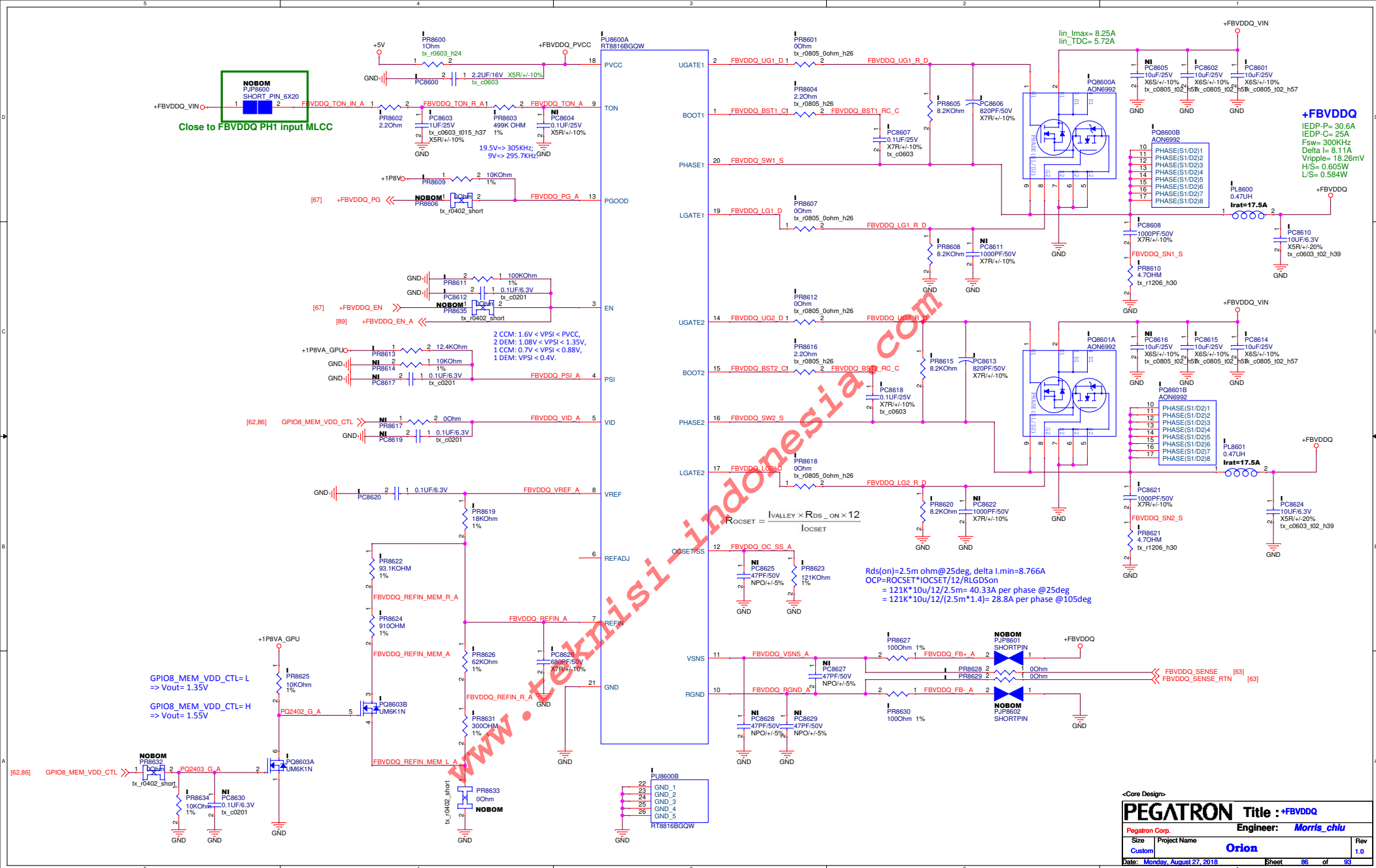
Date: Monday, August 27, 2018 Sheet 63 of 63

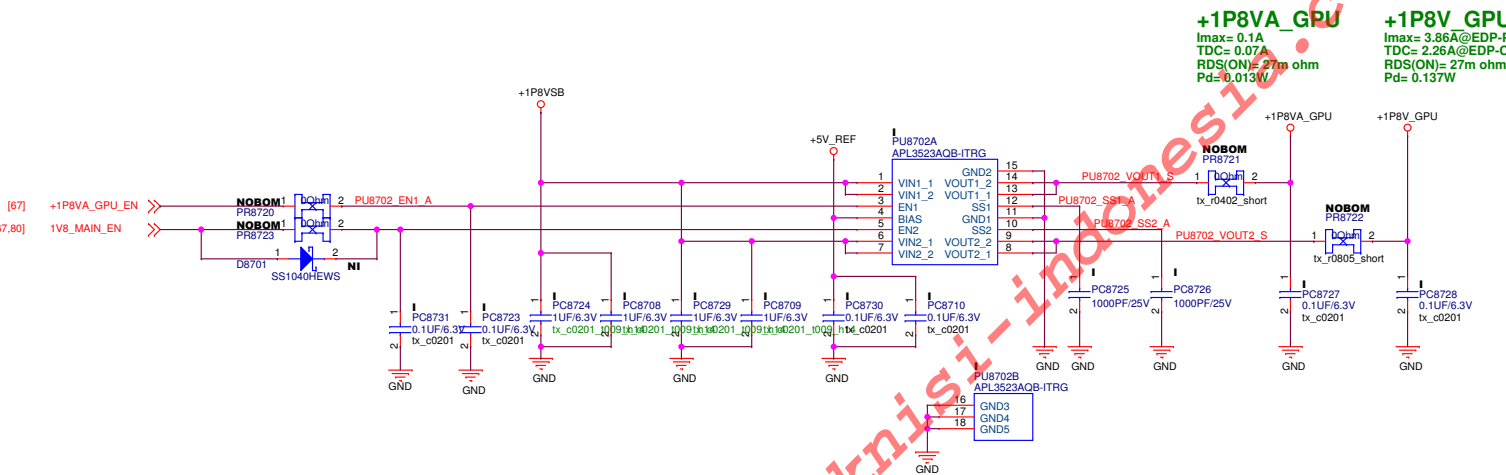
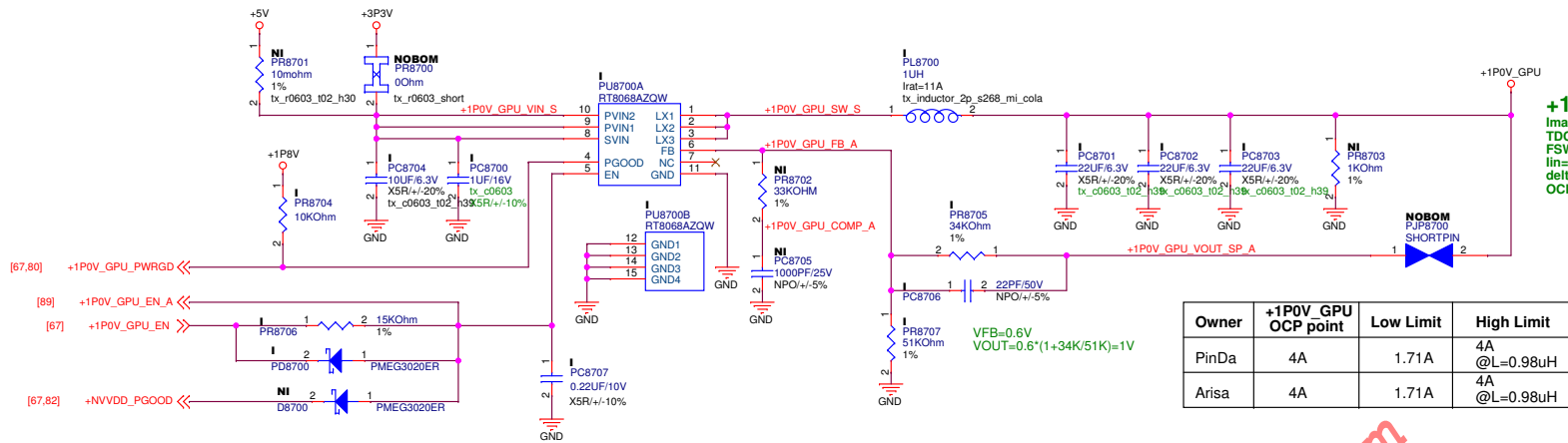


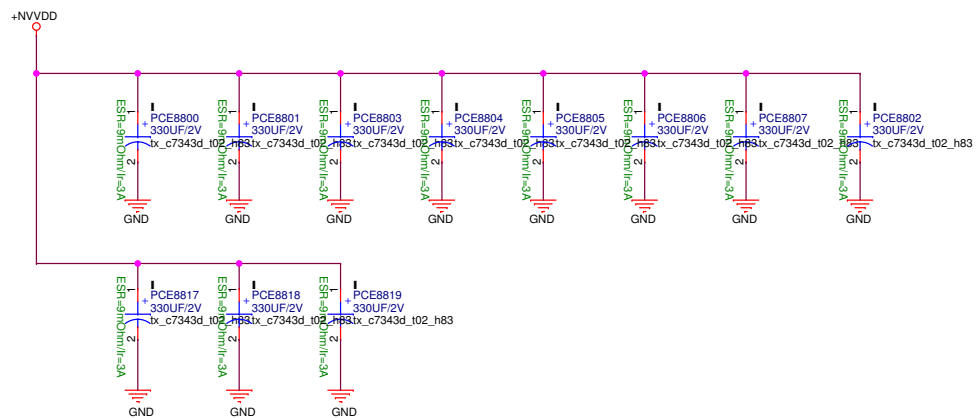
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+NVVDDS(merge to NVVDD)
IEDP-P= 53.7A
IEDP-C= 27A
Fsw= 305KHz
Delta I= 15.68A
Vripple= 35.29mV
H/S= 0.546W
L/S= 0.7W

<Core Design>			
PEGATRON		Title : xxxxxx	
Pegatron Corp.		Engineer: Morris_chiu	
Size	Project Name		Rev
A3	Orion		1.0
Date: Monday, August 27, 2018		Sheet 85 of 93	

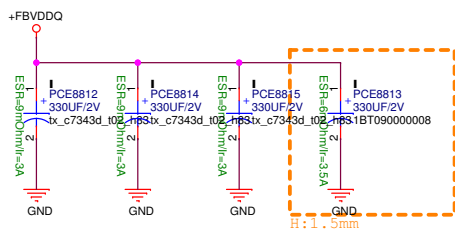






+NVVDD Output CAP(w/ +NVVDDS)

330uF/2V * 8 pcs + 330uF/2V * 3 pcs



+FBVDDQ Output CAP

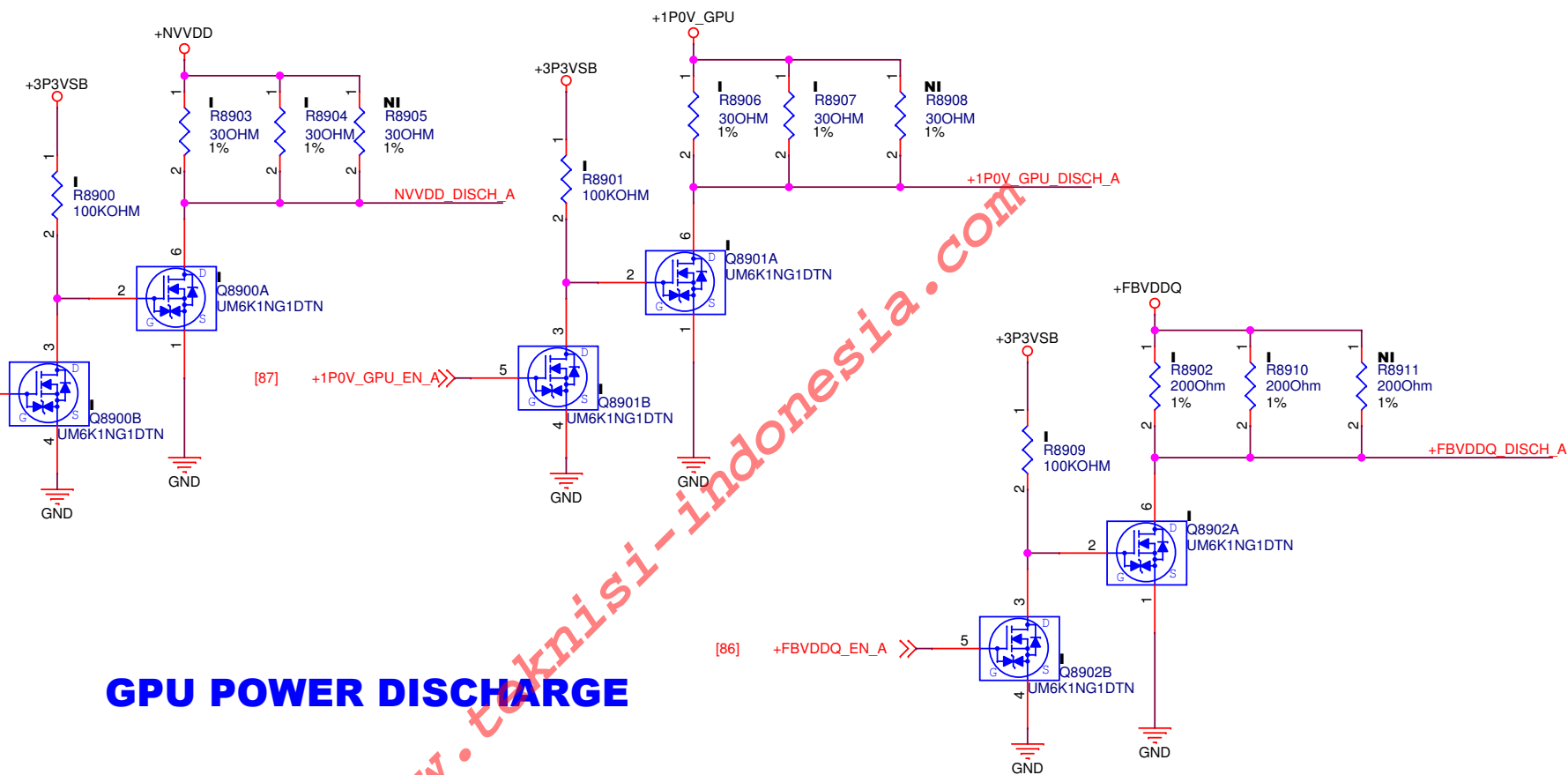
330uF/2V * 4 pcs

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<Core Design>

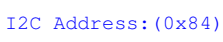
PEGATRON		Title : GPU_POWER_CAP	
Pegatron Corp.		Engineer: Morris_chiu	
Size	Project Name	Orion	Rev
A3			1.0
Date: Monday, August 27, 2016		Sheet	88 of 93

GPU POWER DISCHARGE



<Core Design>

PEGATRON		Title : GPU POWER DISCHARGE	
Pegatron Corp.		Engineer: Morris_chiu	
Size A4	Project Name Orion		Rev 1.0
Date: Monday, August 27, 2018		Sheet 89 of 94	

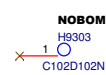
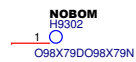
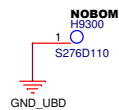
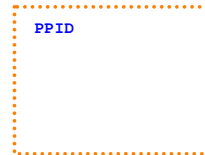
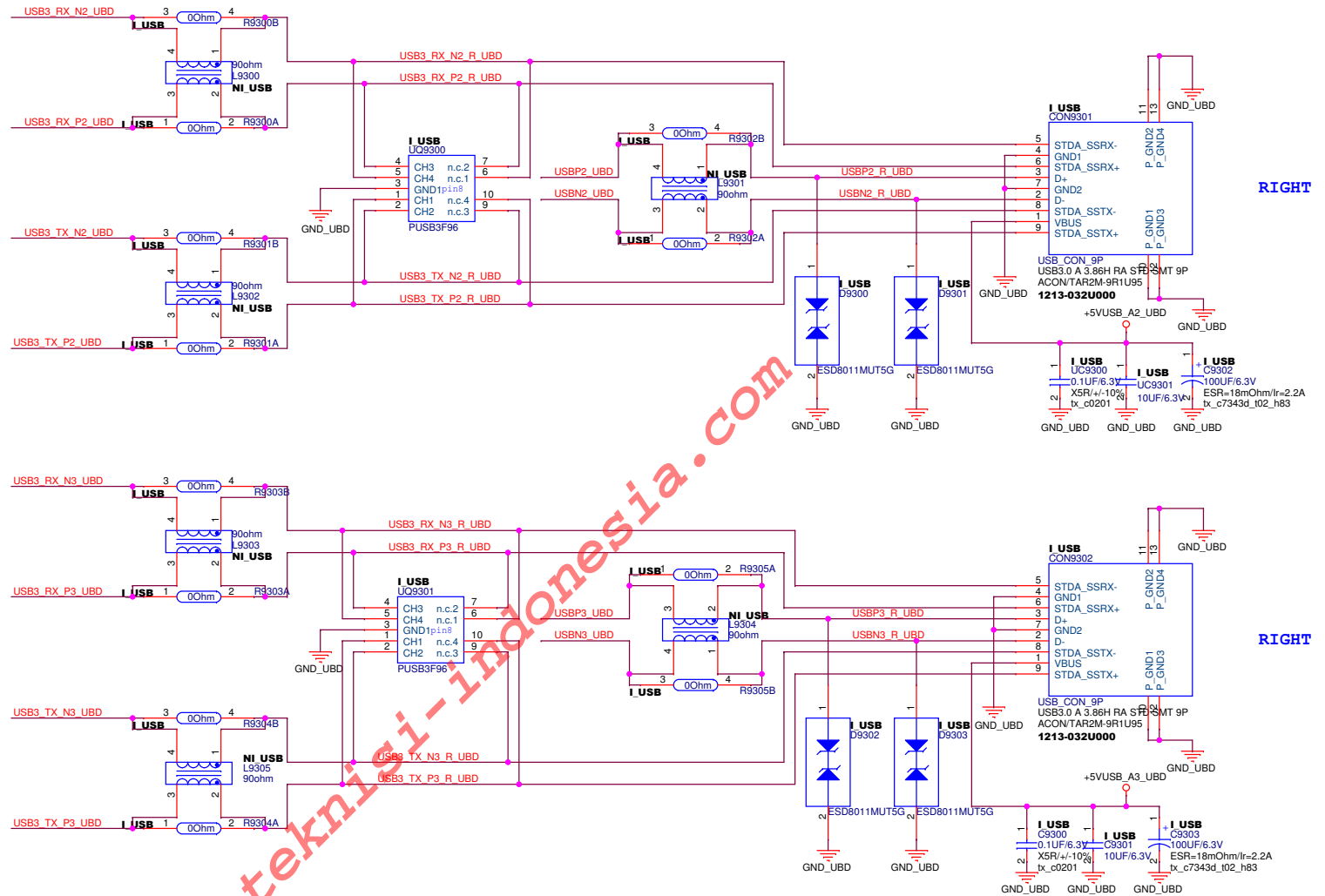
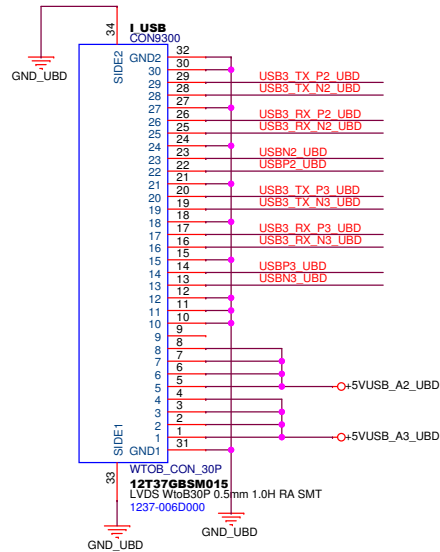


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<Core Design>

PEGATRON		Title : xxxxxx	
Pegatron Corp.		Engineer: <i>Morris_chiu</i>	
Size A4	Project Name Orion		Rev 1.0
Date: Monday, August 27, 2018		Sheet 92	of 93

CARD-USB CON



<Core Design>

PEGATRON		Title : CARD - USB CON	
Pegatron Corp.		Engineer: Morris_chiu	
Size A3	Project Name Orion		Rev 1.0
Date: Monday, August 27, 2018		Sheet	93 of 93